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Performance evaluation and benchmarking of PLL algorithms for grid-connected RES applications

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Abstract: The phase-locked loop (PLL) is the main controller element for the fast and accurate synchronisation and operation of grid-connected renewable energy systems (RESs). It is used to extract the grid voltage information such as the phase angle, the frequency and amplitude. Subsequently, this information is used in the control system of the grid-side converter of the RES. The performance of the PLL is critical under abnormal grid conditions such as in the event of balanced and/or unbalanced faults, frequency and phase variations, the presence of harmonics, interharmonics and DC offset. This study sets out with a benchmarking study of the four latest state-of-the-art PLLs. The PLLs compared are the decoupled dual synchronous reference frame PLL, the decoupling network designed in *αβ*-frame PLL, the enhanced pre-filtering moving average filter type-2 PLL and the harmonic–interharmonic DC-offset PLL. The PLLs are analysed and compared based on their performance, their dynamic response and their computational complexity. The benchmarking concludes with a PLL selection guide depending on the application and other system constraints. Experiments and simulation results are presented to compare and analyse the performance of the selected PLLs.

1 Introduction

The power electronic-based grid-side converter (GSC) technology is the key element for the efficient and reliable integration of the distributed renewable energy systems (RESs) with the grid. The accurate design of the GSC control system plays a vital role in the overall operation of RES under normal and abnormal grid-operating conditions as regulated and demanded by the modern grid codes. The operation of the GSC mainly depends on the proper design of its control system. The control system consists of the synchronisation unit, the inner current controller and the outer active and reactive power (PQ) controller [1] (Fig. 1). The most important module in the GSC control is the synchronisation unit, and it performs the function of extracting the grid voltage information, that is, phase angle, frequency and amplitude. Typically, phase-locked loop (PLL) synchronisation techniques are employed to achieve the monitoring of the grid voltage [2]. The extracted grid voltage information is subsequently used for enabling the desired control of the GSC. The current and PQ controllers are directly influenced by the response of the synchronisation method. Therefore, the behaviour of the PLL is very fundamental for the overall operation of the grid-connected RESs. The PQ controller is responsible for generating the current references based on the set point of active power (P_{ref}) and the DC-link voltage ($V_{\text{DC-ref}}$), as well as on the set point of the desired reactive power (Q_{ref}) and amplitude of the grid voltage at the point of common coupling $V_{\text{PCC-ref}}$. The current controller is then used to track the provided references and enable the injection of high-quality currents. The performance accuracy of the PLL is critical under off-nominal grid conditions such as in the presence of grid voltage harmonics, interharmonics, voltage sags and swells, balanced and unbalanced grid faults, DC offset, frequency variations and phase jumps [3, 4]. Thus, the design of the PLL should be capable of handling the abnormal grid conditions with improved performance, fast-dynamic response, small oscillations/overshoot and with low computational complexity to be feasibly implemented in the embedded microcontrollers of the real-time GSCs.

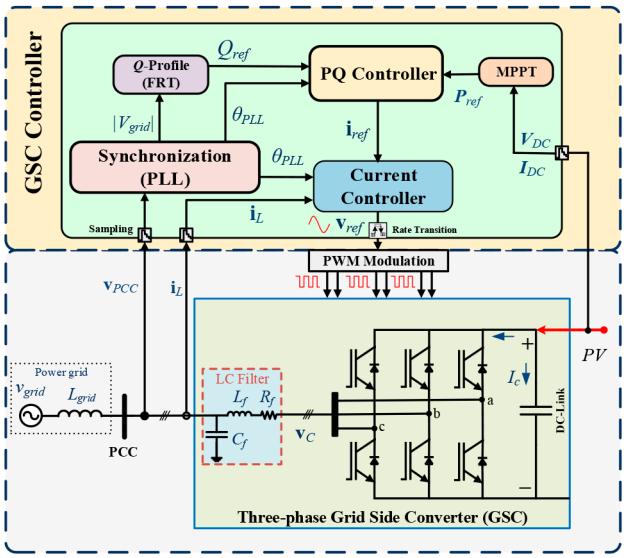

Fig. 1 *Control structure for grid-connected photovoltaic RES system*

The work analyses and compares the four state-of-the-art PLLs based on their performance capabilities, dynamic response and computational complexity. The four PLLs are the decoupled dual synchronous reference frame PLL (ddsrfPLL) [5], the decoupling network designed in *αβ*-frame PLL (DN*αβ*PLL) [4], the enhanced pre-filtering moving average filter type-2 PLL (EPMAF type-2 PLL) [6] and the harmonic–interharmonic DC-offset PLL (HIHDOPLL) [3]. The benchmarking study provides the schematic diagram and a detailed description, the operating principle, the performance capabilities and the advantages and disadvantages of each PLL. The reason for selecting these four PLLs is that three out of four [the DN*αβ*PLL, the EMPAF type-2 PLL and less-complex disturbance rejection (LCDR) PLL] are the most recent developments regarding accurate synchronisation of grid-connected systems under distorted and abnormal grid conditions. The ddsrfPLL is the one, which is commonly referred and used PLL for grid-connected systems under normal grid conditions and faults only. There exist some review studies in the literature

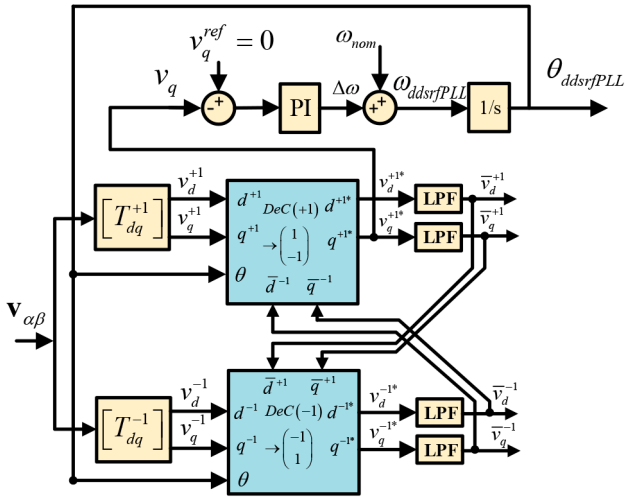

Fig. 2 *Schematic diagram of the ddsrfPLL*

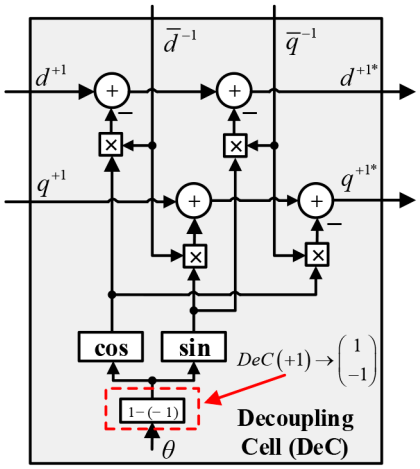

Fig. 3 *Inside structure of a single DeC*

containing various basic and advanced PLLs [2, 7–9]; however, this paper presents a comparison and experimental benchmarking of the most recent state-of-the-art PLLs. The benchmarking carried out in this paper concludes with a selection guide of the most appropriate PLLs depending on the application taking into consideration any specific operating conditions and requirements that could exist.

The details of each PLL are presented in Section 2 and Section 3 discusses the performance capabilities of each PLL, the computational complexity and the Bode analysis. The simulation and experimental benchmarking under various grid-operating conditions is presented in Section 4. Finally, this paper concludes in Section 5.

2 Details of the PLLs investigated

This section presents the details of the four PLLs analysed.

2.1 Decoupled dual SRF PLL

The ddsrfPLL [5] employs two SRFs rotating with two different angular speeds. One SRF is rotating with $+\omega$ speed representing the positive-sequence module and the second SRF is rotating with $-\omega$ for the PLL to deal with the negative sequence. The schematic diagram of the ddsrfPLL is shown in Fig. 2. Each of the SRF transforms the grid voltage $\boldsymbol{v}_{\alpha\beta}$ to the corresponding reference frame $\boldsymbol{v}_{dq}^{+1}$ and $\boldsymbol{v}_{dq}^{-1}$. As per the SRF transformation, if a signal containing more than one frequency component is transformed with specific angular speed, it results in undesired oscillation on the transformed component due to the presence of remaining frequency components [2, 7, 10, 11]. Thus, after the transformation by each SRF, -2ω and $+2\omega$ oscillations are, respectively, observed on the $\boldsymbol{v}_{dq}^{+1}$ and $\boldsymbol{v}_{dq}^{-1}$ voltage vectors. The -2ω oscillations on $\boldsymbol{v}_{dq}^{+1}$ are due to the negative-sequence component transformed with $+\omega$ speed and vice versa, as shown in the equations below:

$$\boldsymbol{v}_{dq}^{+1} = [\boldsymbol{T}_{dq}^{+1}]\boldsymbol{v}_{\alpha\beta} = \underbrace{V^{+}\begin{bmatrix}1\\0\end{bmatrix}}_{\text{dc}-\text{term}} + \underbrace{V^{-}\begin{bmatrix}\cos(-2\omega t)\\ \sin(-2\omega t)\end{bmatrix}}_{\text{oscillating}-\text{term}} \tag{1}$$

$$\boldsymbol{v}_{dq}^{-1} = [\boldsymbol{T}_{dq}^{-1}]\boldsymbol{v}_{\alpha\beta} = \underbrace{V^{-}\begin{bmatrix}1\\0\end{bmatrix}}_{\text{dc}-\text{term}} + \underbrace{V^{+}\begin{bmatrix}\cos(2\omega t)\\ \sin(2\omega t)\end{bmatrix}}_{\text{oscillating}-\text{term}} \tag{2}$$

where $[\boldsymbol{T}_{dq}^{n}]$ given in (3) is the transformation matrix with θ being the PLL angle and $\boldsymbol{v}_{\alpha\beta}$ is calculated by processing the three-phase grid voltage $\boldsymbol{v}_{abc}$ using (4)

$$[\boldsymbol{T}_{dq}^{n}] = \begin{bmatrix}\cos(n\theta) & \sin(n\theta)\\ -\sin(n\theta) & \cos(n\theta)\end{bmatrix} \tag{3}$$

$$\boldsymbol{v}_{\alpha\beta} = \frac{2}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\boldsymbol{v}_{\text{abc}} \tag{4}$$

Consequently, the transformed voltage vectors ($\boldsymbol{v}_{dq}^{+1}$ and $\boldsymbol{v}_{dq}^{-1}$) are provided to the decoupling cells (DeCs) to remove the oscillations and become oscillation-free voltage vectors $\boldsymbol{v}_{dq}^{+1*}$ and $\boldsymbol{v}_{dq}^{-1*}$ as given in (5) and (6). The structure of the DeC is depicted in Fig. 3

$$\boldsymbol{v}_{dq}^{+1*} = \boldsymbol{v}_{dq}^{+1} - [\boldsymbol{T}_{dq}^{+2}]\bar{\boldsymbol{v}}_{dq}^{-1} \tag{5}$$

$$\boldsymbol{v}_{dq}^{-1*} = \boldsymbol{v}_{dq}^{-1} - [\boldsymbol{T}_{dq}^{-2}]\bar{\boldsymbol{v}}_{dq}^{+1} \tag{6}$$

The q-component of the resulting positive-sequence oscillation-free voltage vector $\boldsymbol{v}_{dq}^{+1*}$ is passed through a dqPLL-based phase detector algorithm. The ddsrfPLL performs accurately in the presence of balanced and unbalanced faults, frequency and phase variations, and has faster dynamics. However, it is not immune to grid voltage harmonics, interharmonics and DC offset, and it results in high-frequency overshoot under faults.

2.2 Decoupled network in αβ PLL

The DN$\alpha\beta$PLL is an extension of the ddsrfPLL for eliminating grid harmonics; however, it is designed in the $\alpha\beta$ frame. The DN$\alpha\beta$PLL is immune to grid voltage harmonics and unbalanced faults. The schematic diagram of the DN$\alpha\beta$PLL is shown in Fig. 4, which consists of a decoupling network consisting of various DeCs. The DeCs are pre-defined with specific harmonic or voltage component to be extracted and compensated. Unlike, the ddsrfPLL, the grid voltage is transformed into the selected SRFs and the resulting oscillations on the transformed vectors are decoupled through the respective DeCs. The oscillation-free vectors are obtained as per the mathematical relationship described in (7) and (8), where n is the desired sequence and m represents all the other voltage components contained in the grid voltage. For example, if the voltage is distorted with $+5$th, -7th harmonic and is also unbalanced, for the desired sequence of $+1$, $n = +1$ and $m = +5$, -7

$$\boldsymbol{v}_{\alpha\beta}^{*n} = \left[\boldsymbol{v}_{\alpha\beta} - \sum_{m \neq n}[\boldsymbol{T}_{dq}^{-m}][\boldsymbol{F}(s)][\boldsymbol{T}_{dq}^{m}]\boldsymbol{v}_{\alpha\beta}^{*m}\right] \tag{7}$$

$$\begin{aligned}\boldsymbol{V}_{dq}^{*n} &= [\boldsymbol{T}_{dq}^{n}]\boldsymbol{v}_{\alpha\beta}^{*n}\\ &= [\boldsymbol{T}_{dq}^{n}]\left[\boldsymbol{v}_{\alpha\beta} - \sum_{m \neq n}[\boldsymbol{T}_{dq}^{-m}][\boldsymbol{F}(s)][\boldsymbol{T}_{dq}^{m}]\boldsymbol{v}_{\alpha\beta}^{*m}\right]\end{aligned} \tag{8}$$

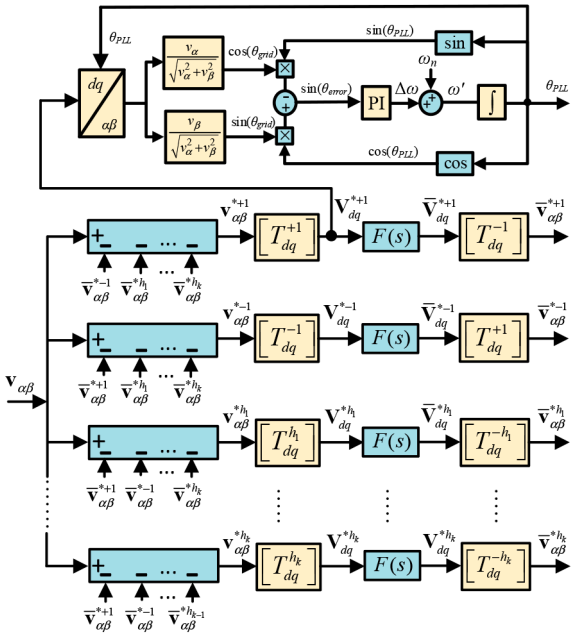

Fig. 4 *Schematic diagram of the DNαβPLL*

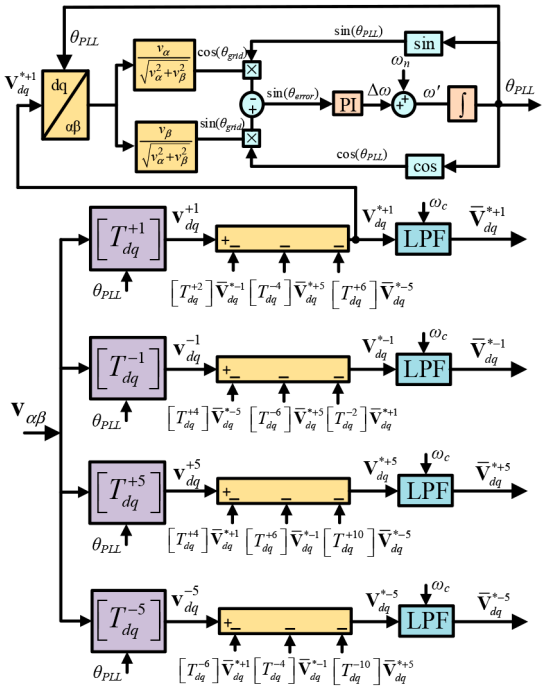

Fig. 5 *Structure of MSHDC PLL for n = + 1, − 2, + 5 and − 5*

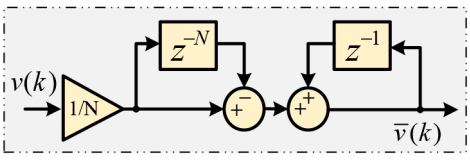

Fig. 6 *Discrete implementation of the MAF*

where $\boldsymbol{F}(s)$ given in (9) represents the low-pass filter (LPF) employed to remove residual oscillations, and the resulting filtered decoupled vectors $(\boldsymbol{v}_{\alpha\beta}^{*m})$ are fed back to enable the decoupling process, as shown in Fig. 3

$$\boldsymbol{F}(s) = \begin{bmatrix} \dfrac{\omega_{\mathrm{cf}}}{s+\omega_{\mathrm{cf}}} & 0 \\ 0 & \dfrac{\omega_{\mathrm{cf}}}{s+\omega_{\mathrm{cf}}} \end{bmatrix} \tag{9}$$

The selection of appropriate cut-off frequency ω_{c} is necessary for enabling the proper subtractions. The optimal value of ω_{cf} for the positive and negative-sequence DeCs is $\omega/\sqrt{2}$ with ω being the nominal fundamental angular grid frequency (in the present case, $\omega = 2\pi 50$ rad/s). In contrast, the ideal value of the cut-off frequency for the harmonic block falls in the range $0.3\omega \leq \omega_{\mathrm{cf}} \leq 0.7\omega$. The DN$\alpha\beta$PLL can eliminate only selected low-order harmonics, and it is important to pre-tune the DeCs based on the prior knowledge of which harmonics are to be compensated. More DeCs are required if more harmonics are to be compensated, increasing in this way the complexity. Furthermore, the DN$\alpha\beta$PLL is not immune to grid voltage interharmonics and DC offset. It is important to mention that the DN$\alpha\beta$PLL is a less-complex version of the originally extended ddsrfPLL named as multi-sequence harmonic DeC PLL (MSHDCPLL) [12] designed in the dq frame, as shown in Fig. 5 and its decoupling capability is mathematically expressed in the equation below:

$$\boldsymbol{V}_{dq}^{*n} = [\boldsymbol{T}_{dq}^{n}]\boldsymbol{v}_{\alpha\beta} - \sum_{m \neq n} \left\{\boldsymbol{T}_{dq}^{(n-m)}\right\} \bar{\boldsymbol{V}}_{dq}^{m} \tag{10}$$

where n is the desired component and m holds for all other values, except n.

The two PLLs are equivalent in performance, but DN$\alpha\beta$PLL has lower complexity. Nevertheless, when compared with the other PLLs, the complexity of DN$\alpha\beta$PLL is still significant for the real-time execution of a GSC controller (as will be demonstrated later in this paper).

2.3 EPMAF type-2 PLL

The MAF-based PLLs are suitable for applications, where complexity is of major concern due to the extremely low computational burden of the MAF. The discrete implementation of the MAF requires only one multiplication, one addition and one subtraction [13, 14], as shown in Fig. 6. The conventional MAFPLL [14] (shown in Fig. 7) presents, however, slower dynamic response, complicated tuning procedures, inaccurate phase angle extraction and inaccurate harmonic–interharmonic mitigation under off-nominal grid frequencies. Recently, an EPMAF type-2 PLL has been proposed in [6] to deal with the aforementioned issues. The structure of the EPMAF type-2 is shown in Fig. 8. This PLL addresses the problems of conventional MAFPLL by shifting the MAF and the phase error compensation to the pre-filtering stage. The grid voltage is transformed to SRF^{+1} frame and is subsequently passed through the MAF to remove the oscillating terms contained in the $\boldsymbol{v}_{dq}$. However, the phase angle of the filtered signal $\bar{\boldsymbol{v}}_{dq}$ is compromised of the filter response and results in a phase drift of $-\Delta\omega k_{\varphi}$ in the equation below:

$$\bar{\boldsymbol{v}}_{dq} = |\bar{\boldsymbol{v}}_{dq}| \mathrm{e}^{\left(-\Delta\omega(T_{\omega}-T_{\mathrm{c}})/2\right)} \tag{11}$$

where $\Delta\omega = \omega_{\mathrm{g}} - \omega_{\mathrm{nf}}$ denotes the error of the actual (ω_{g}) and nominal (ω_{nf}) grid frequency; T_{c} represents the sampling period; $T_{\omega} = NT_{\mathrm{c}}$ is the window length of MAF; and N is the number of samples within the window [6, 14, 15].

The output of the MAF is corrected in phase by applying for the phase error compensation and is then passed to the phase detector stage of the PLL. As per the EPMAF type-2 PLL, the error in the phase angle is removed by transforming back the filtered $\bar{\boldsymbol{v}}_{dq}$ with the same amount of drift added to the nominal phase angle for reverse transformation, that is, the reverse transformation from dq to $\alpha\beta$ is carried out with an angle given in the equation below:

$$\theta_{dq2\alpha\beta} = \theta_{\mathrm{nf}} + \left(-\Delta\omega k_{\varphi}\right) \tag{12}$$

where $\theta_{\mathrm{nf}} = \int_{\mathrm{nf}}^{\omega} \mathrm{d}t$ with ω_{nf} being the nominal grid frequency ($2\pi 50$ rad/s, for example).

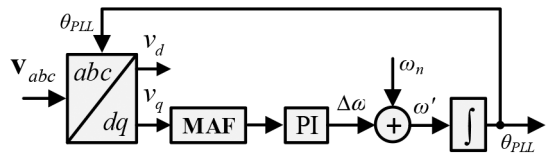

Fig. 7 *Block diagram of the conventional MAF*

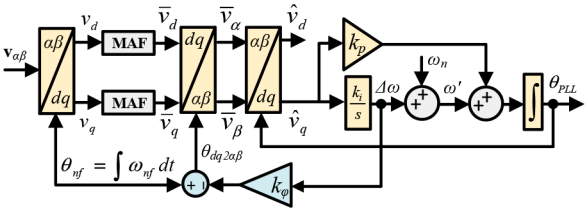

Fig. 8 *Schematic diagram of the enhanced pre-filtering stage type-2 PLL (EPMAF type-2 PLL)*

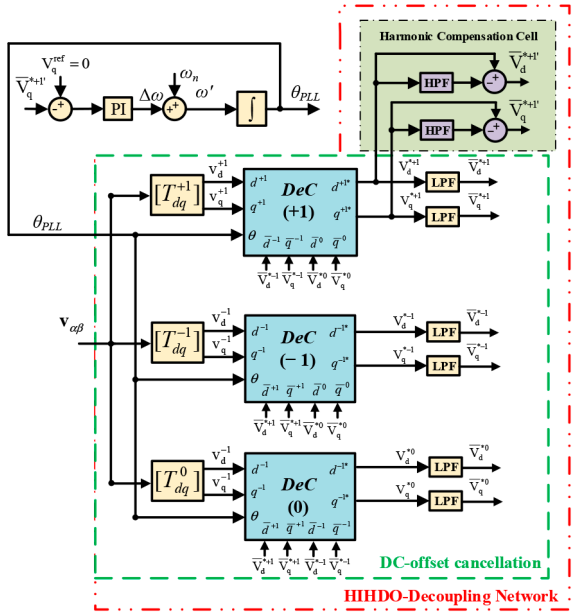

Fig. 9 *Schematic diagram of the HIHDOPLL*

The EPMAF type-2 PLL improves the dynamic response of the conventional MAF, but compared with the other non-MAFPLLs, it is still slower. There is a clear trade-off between complexity and dynamic response. The settling time of the EPMAF type-2 is typically 200% of the time taken by the non-MAF PLLs analysed in this paper. Also, it can compensate for the DC offset only if the MAF window length is set to 0.02 s.

2.4 Harmonic–interharmonic DC-offset PLL

The HIHDOPLL [3] can compensate for grid voltage harmonics, interharmonics, DC offset and unbalance with a faster dynamic response. It employs a novel mathematic cancellation DeC for the effective mitigation of DC offset and negative sequence of the grid voltage. Besides, a simple yet effective, harmonic–interharmonic compensation network is used to eliminate the higher-frequency oscillations generated by the grid harmonics and interharmonics, as shown in Fig. 9. The grid voltage is passed through the mathematic DeC [given in (13)] for the fast and accurate mitigation of negative sequence and DC offset

$$\begin{bmatrix} \boldsymbol{V}_{dq}^{*+1} \\ \boldsymbol{V}_{dq}^{*-1} \\ \boldsymbol{V}_{dq}^{*0} \end{bmatrix} = \begin{bmatrix} \boldsymbol{v}_{dq}^{+1} \\ \boldsymbol{v}_{dq}^{-1} \\ \boldsymbol{v}_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & \left[\boldsymbol{T}_{dq}^{+1-(-1)}\right] & \left[\boldsymbol{T}_{dq}^{+1-(0)}\right] \\ \left[\boldsymbol{T}_{dq}^{-1-(+1)}\right] & [0] & \left[\boldsymbol{T}_{dq}^{+1-(0)}\right] \\ \left[\boldsymbol{T}_{dq}^{0-(+1)}\right] & \left[\boldsymbol{T}_{dq}^{0-(-1)}\right] & [0] \end{bmatrix} \begin{bmatrix} \bar{\boldsymbol{V}}_{dq}^{*+1} \\ \bar{\boldsymbol{V}}_{dq}^{*-1} \\ \bar{\boldsymbol{V}}_{dq}^{*0} \end{bmatrix} \quad (13)$$

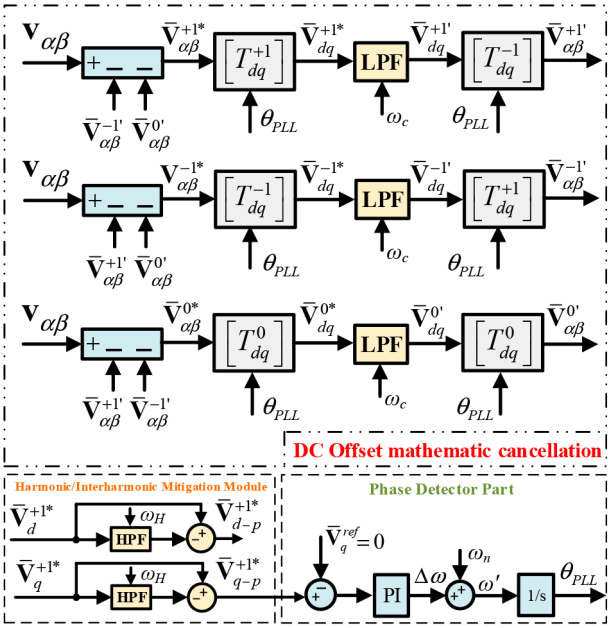

Fig. 10 *LCDRPLL*

where $\bar{\boldsymbol{V}}_{dq}^{*n} = F(s)\boldsymbol{V}_{dq}^{*n}$ is the filtered estimated voltage vector. The selection of the cut-off frequency is different for each component. For positive and negative sequences, $\omega/\sqrt{2}$ is the optimal cut-off value, whereas a lower cut-off frequency (ω/4.5) is required for the extraction of the DC component $\boldsymbol{V}_{dq}^{*0}$ [16]. The lower cut-off frequency is necessary because the cross-coupling positive and negative sequences responsible for the oscillations generated on the DC vectors are the most dominant grid voltage components.

The estimated positive-sequence voltage vector $\boldsymbol{V}_{dq}^{+1*}$ compensated for the unbalance and DC offset obtained from the DeCs is subsequently passed through the harmonic compensation network (HCN) for the effective mitigation of harmonics and interharmonics as shown in (14). Finally, the q-component of the resulting vector $\bar{\boldsymbol{V}}_{dq}^{*+1}$ is passed to the phase detector part of the PLL to extract the phase and frequency

$$\bar{\boldsymbol{V}}_{dq}^{*+1} = \boldsymbol{V}_{dq}^{*+1} - \underbrace{\begin{bmatrix} \frac{s}{s+\omega_H} & 0 \\ 0 & \frac{s}{s+\omega_H} \end{bmatrix}}_{\text{HPF}} \boldsymbol{V}_{dq}^{*+1} \quad (14)$$

The appropriate range for the cut-off frequency (ω_H) of the high-pass filter, considering both accuracy and faster dynamic response, lies in the range $0.2\omega \leq \omega_H \leq 0.45\omega$ [3].

The HIHDOPLL does not require prior knowledge of which harmonics–interharmonics to be compensated and presents faster dynamic response. Its compensation is not limited to specific low-order harmonics and can compensate any harmonics–interharmonics present in the grid. It has lower computational complexity compared with the aforementioned non-MAF PLLs. However, since the dq-rotating reference frame is mainly used to design the HIHDOPLL, it still requires a large number of Park's transformations, ultimately increasing the complexity for real-time GSC controller. Recently, the HIHDOPLL has been modified as an LCDRPLL [17] that offers lower complexity with performance capabilities similar to those of the HIHDOPLL. The main contribution of LCDRPLL is the development of a less-complex mathematics-based DC-offset mitigation module in the stationary reference frame. The block diagram of the LCDPLL is shown in Fig. 10. The mathematical equation governing the development of LCDRPLL is given in the equation below:

$$\bar{V}_{dq}^{n*} = \left[T_{dq}^{-n}\right]\underbrace{\left(v_{\alpha\beta} - \sum_{m \neq n} \bar{V}_{\alpha\beta}^{m'}\right)}_{\bar{V}_{\alpha\beta}^{n*}} \quad (15)$$

The $\bar{V}_{dq}^{+1*}$ obtained from (15) is transferred to the HCN [similar to the one expressed in (14)] for the removal of oscillations caused by harmonics–interharmonics. The resulting $\bar{V}_{q-p}^{+1*}$ is transferred to the phase detector part of the PLL to obtain the required phase and frequency. Thus, the LCDRPLL can work under unbalanced faults, harmonics, interharmonics and DC offset in the grid voltage with reduced computational complexity and faster dynamic response. On the basis of the performance capabilities, faster dynamic response and lower complexity, it can be concluded that the LCDRPLL is the most advanced and less-complex PLL.

3 Comparison of computational complexity and performance capabilities

The computational complexity analysis and performance capabilities of the various PLLs are presented in Table 1. The performance is investigated and summarised for various indices such as the dynamic response, the operation of PLLs under distorted grid conditions, the overshoot in the estimated phase/frequency, the PLL response to frequency variations and operation to three-phase faults (blackout). To investigate the complexity, two approaches are used. The first one addresses the complexity by experimentally measuring the processing time required by each PLL using the Texas Instrument TMS320F28335 microcontroller. This microcontroller is widely used for such power electronic applications. The time taken by the PLL algorithm to execute/run within a given sampling period of the embedded microcontroller is referred to as the processing time. For the real-time execution of the microcontroller, the processing time of the whole GSC controller (which includes the PLL and other control peripherals) must be less than the given sampling period. It is, therefore, necessary to design such control peripherals with the least computational burden as possible. The other approach considers the number of mathematical operations (such as the subtractions, additions and multiplications) required by each PLL within each control loop.

The ddsrfPLL requires less computational resources among non-MAFPLLs. However, it is not immune to distorted grid conditions. The DN$\alpha\beta$PLL and MSHDCPLL present equivalent performance, except that the former has lower complexity. The major drawback of the DN$\alpha\beta$PLL is that it still presents significant complexity compared with the other PLLs and is immune only to selected harmonics. Furthermore, it has high overshoot and inaccurate response under severe three-phase faults. Among the MAFPLLs, EPMAF type-2 has superior performance, but slower dynamics. Considering the overall capabilities of the LCDRPLL, it is the most advanced, fastest and less-complex PLL. Its major advantage is that it can compensate for any harmonics and interharmonics present in the grid with faster dynamic response and without requiring any prior knowledge.

The performance of the PLLs for mitigating the undesired components and passing the required 50 Hz is demonstrated by the respective Bode plots (Fig. 11). It is worth mentioning that the transfer functions are expressed in the $\alpha\beta$ frame to visualise the effect of the PLL on the frequency components in the actual sinusoidal domain. The transfer function for the ddsrfPLL is given in (16), and corresponding Bode analysis is shown in Fig. 11 (black line). The ddsrfPLL considers mitigating only the negative sequence of grid voltage, and all the other components are passed with unity gain

$$\frac{\bar{V}_{\alpha\beta}^{*+1}}{v_{\alpha\beta}} = \left[\frac{1 - \left(\mathrm{TLPT}^{-1}\right)}{1 - \mathrm{TLPT}^{+1}.\left(\mathrm{TLPT}^{-1}\right)}\right] \quad (16)$$

Table 1 Computational complexity and performance comparison of the various PLLs

PLL techniques	Computational complexity investigation		Accurate operation under	Settling time under fault	Frequency/phase overshoot	Operation under non-nominal frequency	Performance under three-phase fault (blackout)
	Experimental processing time (TMS320F28335 microcontroller), μs	Total mathematical operations					
ddsrfPLL	14.4	8 subtractions, 8 additions, 32 multiplications	unbalance only	low	high	accurate	accurate
DN$\alpha\beta$PLL	88	200 subtractions, 40 additions, 160 multiplications	unbalance, selected harmonics	high	high	accurate	inaccurate
MSHDCPLL	296	280 subtractions, 120 additions, 640 multiplications	unbalance, selected harmonics	high	high	accurate	inaccurate
MAFPLL	5.5	3 subtractions, 8 additions, 11 multiplications	unbalance, harmonics–interharmonics[a], DC offset[b]	very high	low	inaccurate	lethargic
EPMAF type-2 PLL	11.6	6 subtractions, 10 additions, 25 multiplications	unbalance, harmonics–interharmonics, DC offset[a]	high	low	accurate	lethargic
HIHDOPLL	31.6	17 subtractions, 19 additions, 70 multiplications	unbalance, any harmonics–interharmonics, DC offset	low	low	accurate	accurate
LCDRPLL	20.1	9 subtractions, 12 additions, 45 multiplications	unbalance, any harmonics–interharmonics, DC offset	low	low	accurate	accurate

[a]Cannot fully compensate harmonics–interharmonics under off-nominal frequency.

[b]Compensate DC offset only when $T_{\omega} = 0.02$ s. Note: in the context of control processes in this work, a low settling time ranges from 20 to 30 ms, whereas the high settling time range is from 50 to 100 ms.

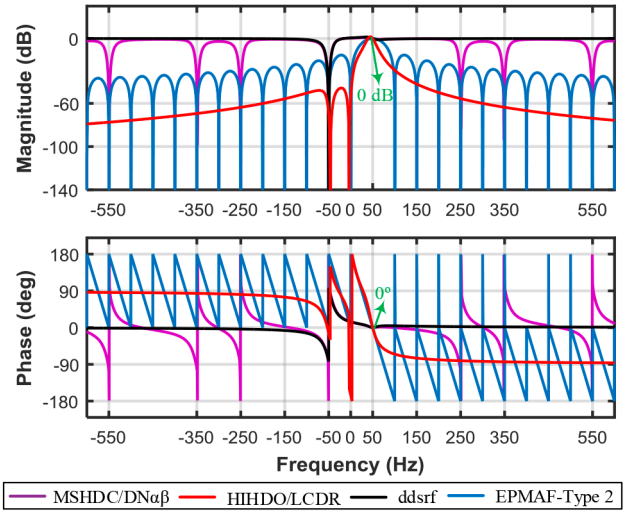

Fig. 11 *Bode diagram of the ddsrfPLL, EPMAF type-2 PLL, MSHDC/DNabPLL and HIHDO/LCDRPLL*

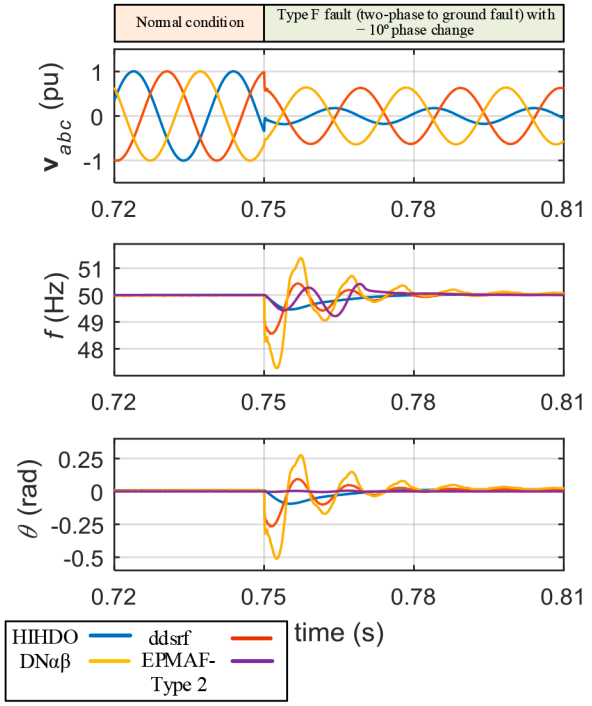

Fig. 12 *Performance comparison of the four PLLs under an unbalanced type-F fault*

The TLPT^{m} represents the complex-frequency-domain transfer function for forward and reverse transformation of a signal passing through the LPF. It is obtained by converting the Park's transformation matrices to corresponding Euler representation followed by Laplace shifting operation [1] and is given as:

$$\mathrm{TLPT}^{m} = \left[\boldsymbol{T}_{dq}^{-m}\right][\mathrm{LPF}]\left[\boldsymbol{T}_{dq}^{m}\right] = \frac{\omega_{\mathrm{cut}\_m}}{s + (\omega_{\mathrm{cut}\_m} - \mathrm{j}\cdot m\cdot\omega)} \tag{17}$$

where ω is the nominal grid frequency and ω_{cut_m} is the cut-off frequency of LPF associated with the mth frequency component. For ddsrfPLL, the cut-off frequency is $\omega/\sqrt{2}$.

Furthermore, the transfer function for the MSHDCPLL and DN$\alpha\beta$PLL is shown in (18) for $n = +1, -1, +5, \ldots, -13$ and the Bode analysis is depicted in Fig. 11 (purple line). The transfer characteristics for both MSHDC and DN$\alpha\beta$ are exactly equivalent. It can be seen that these PLLs can mitigate only the selected low-order harmonics. However, the interharmonics, unselected harmonics and DC component (0 Hz) are passed with unity gain and zero-phase shift

$$\frac{\tilde{\boldsymbol{V}}_{\alpha\beta}^{*+1}}{\boldsymbol{v}_{\alpha\beta}} = \left[\frac{1 - \left(\mathrm{TLPT}^{-1} + \mathrm{TLPT}^{-5} + \cdots + \mathrm{TLPT}^{-13}\right)}{1 - \mathrm{TLPT}^{+1}\cdot\left(\mathrm{TLPT}^{-1} + \mathrm{TLPT}^{-5} + \cdots + \mathrm{TLPT}^{-13}\right)}\right] \tag{18}$$

The performance capabilities of HIHDOPLL and LCDRPLL are equivalent, and thus, the two can be represented by the transfer function given in (19). The corresponding Bode analysis shows that these two PLLs offer a better compensation capability (larger negative gains and phase shift) compared with the other PLLs, and also they can compensate for DC offset and any harmonic–interharmonic present in the grid voltage

$$\underbrace{\frac{\tilde{\boldsymbol{V}}_{\alpha\beta}^{*+1'}}{\boldsymbol{v}_{\alpha\beta}}}_{\text{HIHDO}} = \underbrace{\frac{\tilde{\boldsymbol{V}}_{\alpha\beta\cdot p}^{+1*}}{\boldsymbol{v}_{\alpha\beta}}}_{\text{LCDR}} = \underbrace{\left[\frac{1 - \left(\mathrm{TLPT}^{-1} + \mathrm{TLPT}^{0}\right)}{1 - \mathrm{TLPT}^{+1}\cdot\left(\mathrm{TLPT}^{-1} + \mathrm{TLPT}^{0}\right)}\right]}_{\text{for DC offset network}} \cdot \underbrace{\left(1 - \left[\boldsymbol{T}_{dq}^{-1}\right][\mathrm{HPF}]\left[\boldsymbol{T}_{dq}^{+1}\right]\right)}_{\text{for HCN}} \tag{19}$$

The transfer characteristics of the EPMAF type-2 PLL given in (20) and are graphically depicted in Fig. 11 (blue line). The integer multiples of the inverse window length ($1/T_{\omega}$) are completely blocked by the MAF and the remaining harmonics–interharmonics are not as well compensated as with the LCDR and HIHDOPLLs. For example, the gain in dB at 174 Hz for LCDRPLL and EPMAF type-2 are, respectively, equal to − 57.95 and − 26.46 dB

$$\frac{\tilde{\boldsymbol{v}}_{\alpha\beta}}{\boldsymbol{v}_{\alpha\beta}} = \frac{1 - \mathrm{e}^{-T_{\omega}(s - \mathrm{j}\omega_{\mathrm{nf}})}}{T_{\omega}(s - \mathrm{j}\omega_{\mathrm{nf}})} \tag{20}$$

4 Results and discussion

This section presents the simulation and experimental tests carried out for the selected PLLs. The PLLs are tuned based on the methods presented in Section 6, and all the PLLs are analysed for similar tuning parameters.

4.1 Simulation results

The selected PLLs are developed in the MATLAB/Simulink and tested under various grid conditions. The grid conditions chosen for the performance evaluation are the unbalanced grid faults, frequency/phase variations and the presence of harmonics–interharmonics and DC offset in the grid voltage.

The first test compares the performance of the PLLs to a normal and unbalanced type-F fault (Fig. 12). Initially, the grid voltage is balanced until 0.75 s. At this time, a two phase-to-ground fault (propagated as type-F fault) occurs. The DN$\alpha\beta$PLL has the highest

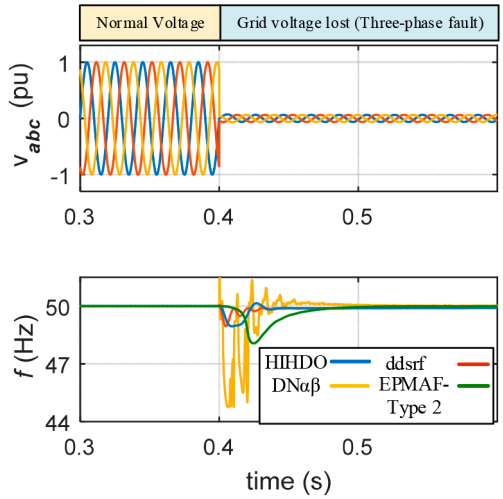

Fig. 13 *Performance comparison of the selected PLLs under three-phase grid fault (blackout)*

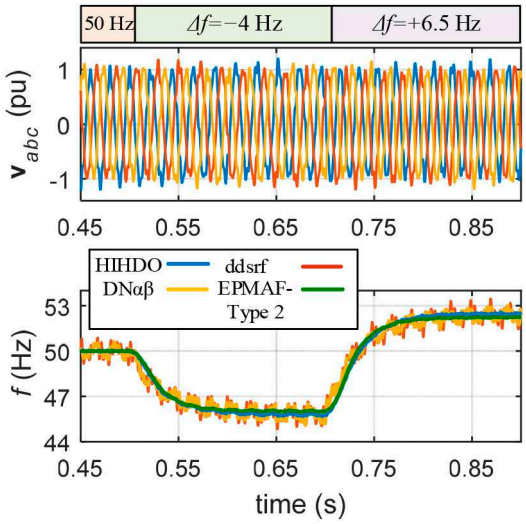

Fig. 14 *Performance comparison of the PLLs under grid frequency variations in the presence of severe distorted grid conditions*

frequency and phase overshoot, whereas the lowest overshoot is experienced by the HIHDOPLL. The EPMAFPLL type-2 presents a slower dynamic response as it takes 30 ms for estimating the grid frequency. The DN$\alpha\beta$PLL also presents large settling time because it has higher overshoot and more oscillations.

The PLLs are further analysed for the case when the grid voltage becomes nearly zero (Fig. 13). This might occur because of a three-phase-to-ground fault or blackouts. With a balanced three-phase voltage until 0.75 s, the grid voltage is subjected to a three-phase-to-ground fault with 95% voltage sag at 0.75 s. The DN$\alpha\beta$PLL suffers from large oscillations at the time of the fault, and it takes more time to settle. In addition to DN$\alpha\beta$PLL, the EPMAF type-2 PLL has a slower dynamic response. Among ddsrfPLL and HIHDOPLL, both PLLs present similar responses along with the same overshoot and settling time.

The PLLs are also tested for the case of frequency variation in the presence of harmonics–interharmonics and DC offset (Fig. 14). The conditions are as follows:

- Harmonics: 6.5% of 5th and 5.5% of 7th.
- Interharmonics: 3.5% of 3.4th and 4% of 5.6th.
- DC offset: 6, 4 and 5.2% per phase.

The DN$\alpha\beta$PLL is not immune to interharmonics and DC offset, whereas the ddsrfPLL is susceptible to harmonics, interharmonics and DC offset. Thus, both DN$\alpha\beta$PLL and ddsrfPLL result in inaccurate frequency estimation. On the other hand, the HIHDOPLL and the EPMAF type-2 PLL mitigate for these

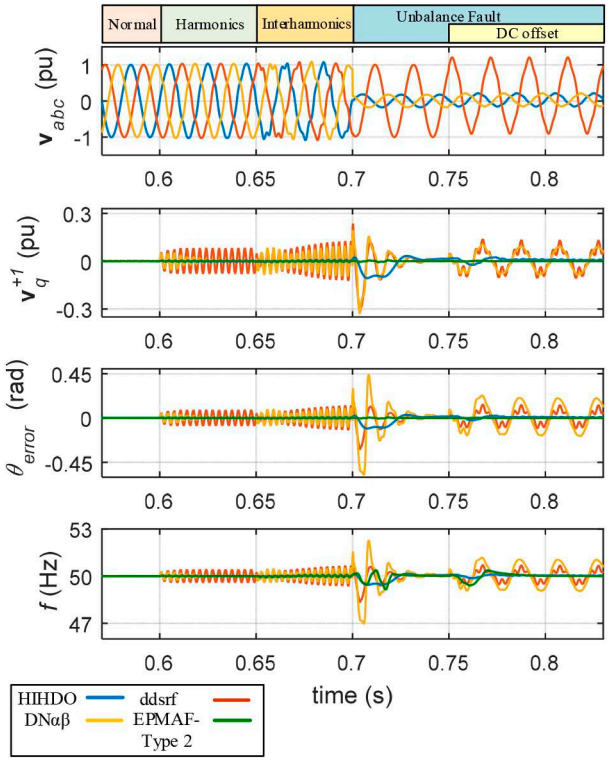

Fig. 15 *Performance comparison of the selected PLLs under various abnormal grid conditions*

abnormal conditions and result in accurate frequency estimation. However, the EPMAF type-2 PLL has a slower dynamic response between the two.

The next case study tests the PLLs under various normal and abnormal grid conditions such as harmonics, interharmonics, faults and DC offset, all occurring consecutively (Fig. 15). The grid quantities estimated from the PLLs are the q-axis grid voltage, the phase error and the grid frequency. Initially, until 0.6 s, the grid voltage is balanced and harmonic free, to which all the four PLLs respond accurately. However, at 0.6 s, 5% of the -5th harmonic and 2.5% of the 7th harmonic are injected in the grid voltage. The HIHDOPLL, the EPMAF type-2 PLL and the DN$\alpha\beta$PLL are immune to these harmonics, and they result in accurate performance.

On the other hand, the ddsrfPLL results in undesired oscillations in the estimated quantities as it cannot perform under harmonics. At 0.65 s, the grid voltage is distorted with 7.3th and 5.4th interharmonics with a magnitude of 4 and 8%, respectively. Both DN$\alpha\beta$PLL and ddsrfPLL are unable to respond accurately. The HIHDOPLL and EPMAF type-2 PLLs, on the other hand, cancel out the oscillations caused by interharmonic distortion and precisely estimate the phase angle and frequency of grid voltage. Furthermore, an unbalanced fault occurs at 0.7 s, and the HIHDOPLL results in lower-frequency overshoot and faster settling time, whereas the DN$\alpha\beta$PLL and the ddsrfPLL suffer from higher overshoots in both estimated frequency and phase. At 0.75 s, 15% DC offset and 5.5% -5th harmonic is modulated on the grid voltage, and it becomes DC shifted and distorted. Both EPMAF type-2 and HIHDOPLLs work precisely under this disturbance by fast and accurate mitigation of DC offset and harmonic distortion.

Concluding, the selection of PLL is a trade-off between the complexity and the dynamic response. If the dynamic response of the PLL is of major concern, the HIHDOPLL is an ideal solution. On the other hand, if computational complexity is of major concern and slower dynamic response is not a problem, the EPMAF type-2 PLL is a better candidate. Also, if the grid voltage is free of harmonic distortion, and the only concern is for unbalanced faults, the ddsrfPLL is a better choice as it has a faster dynamic response.

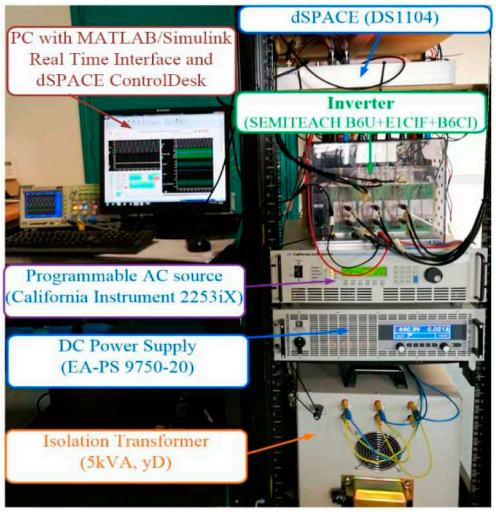

Fig. 16 *Experimental laboratory setup*

4.2 Experimental results

The PLLs are compared and analysed experimentally in the laboratory under various grid conditions. The experimental setup is shown in Fig. 16. The PLL algorithms developed in MATLAB are investigated using the dSPACE-1104 along with a graphical user interface-based real-time control desk. The California Instrument 2253iX three-phase programmable device is used as an AC source to emulate the various grid voltage conditions such as voltage faults, the presence of harmonics and frequency variations. The behaviour of the RES is emulated by an ELEKTRO-AUTOMATIK (EA-PS-9750–20) DC source, and the SEMITEACH (B6U + E1CIF + B6CI) inverter is used as a GSC.

The various grid conditions considered for the experimental benchmarking are the phase change, the harmonic and interharmonic distortions, the frequency variation and a voltage sag event. The point of disturbance in all the experiments is marked with a white arrow labelled with the respective type of disturbance.

The first experimental benchmarking of the four PLLs investigates their responses in the event of a phase change. With zero initial phase angle, the grid voltage is subject to a phase change of $-20°$, and the corresponding responses are presented in Fig. 17 (i). The ddsrfPLL and the DN$\alpha\beta$PLL present higher frequency and phase overshoots, and a minimum overshoot of 0.9 Hz and 0.04 rad is observed for the EPMAF type-2 PLL. The ddsrfPLL presents slower dynamics when compared with the DN$\alpha\beta$/MSHDCPLL and HIHDO/LCDRPLL. Among all, however, and as expected, the EPMAF type-2 has the slowest dynamic response of around 119 ms (for frequency).

The response of the PLLs in the presence of grid voltage harmonics is presented in Fig. 17 (ii). The clean three-phase voltage is distorted with -5th and $+7$th harmonics with a magnitude of 7% concerning the fundamental frequency component. The ddsrfPLL cannot compensate for grid harmonics as observed by the oscillations in both frequency (1.4 Hz peak) and phase error (0.16 rad peak). The remaining three PLLs are immune to harmonic distortions. However, the DN$\alpha\beta$PLL presents oscillations in the start with a maximum peak of 1.2 Hz in frequency and 0.12 rad in θ_{error}. It, therefore, requires more settling time when compared with the PLLs in Figs. 17*e*.

Subsequently, the PLLs are investigated in the presence of -6.7th and 5.4th grid interharmonics [Fig. 17 (iii)]. It can be seen that the DN$\alpha\beta$PLL and ddsrfPLL are not immune to interharmonics, and both suffer from unwanted oscillations. The maximum peak of the frequency and phase error oscillations for the DN$\alpha\beta$PLL are, respectively, equal to 1.48 Hz and 0.19 rad, and for ddsrfPLL these values are 1.45 Hz and 0.18 rad, respectively.

Ultimately, the PLLs are also investigated for a 30% voltage sag event. The responses of the PLLs to this event are depicted in Fig. 18 (i). The DN$\alpha\beta$PLL presents a higher frequency and phase error overshoot of ∼1.95 Hz and 0.2 rad. On the one hand, the frequency overshoot and settling time for the ddsrfPLL and the LCDRPLL are almost the same with the LCDRPLL requiring 25 ms more to settle back after the sag is applied. It is important to note that the amplitude measurements are also included for the EPMAF type-2 and the non-MAF LCDRPLL to emphasise that the MAF takes more time in estimating the grid voltage amplitude as compared with the non-MAF PLLs.

Finally, the response of the PLLs to a step change in the frequency is investigated and presented in Fig. 18 (ii). Initially, the frequency of three-phase voltage is 50 Hz, which, however, is changed to 48.5 Hz at the point marked in Fig. 18 (ii). All the PLLs are capable of tracking the change in frequency, but with different dynamic responses. The higher settling time is observed for EPMAF type-2 PLL, which takes ∼164 ms to reach at 48.5 Hz. The fastest dynamic response is presented by the LCDRPLL, which takes 100 ms to arrive and settle at the reference frequency.

Concluding, the LCDRPLL is immune to grid voltage harmonics, interharmonics, presents lower-phase/frequency overshoot, has faster dynamics and all of the above capabilities with lower complexity (when compared with non-MAF PLLs). On the other hand, the EPMAF type-2 PLL is more suitable when very low complexity is necessary and when a trade-off can be made with the dynamic response.

5 Conclusions

This paper sets out with a benchmarking of four of the latest state-of-the-art PLLs. They are analysed and compared based on their performance capabilities, dynamic response and computational complexity. The detailed description, the analysis, the operating principle, the performance capabilities and the advantages and disadvantages of each PLL have been presented and validated using simulation and experimental results. Three of the PLLs computationally and experimentally investigated are non-MAF-based PLLs, and one incorporates an MAF based. The results demonstrate the superiority of the LCDRPLL. It is the most advanced in terms of capabilities and offers the lowest complexity relative to its capabilities. Modern grid codes require that PLLs respond accurately and with low settling times to the various grid faults, disturbances and conditions such as balanced/unbalanced faults, the presence of harmonics–interharmonics and DC offset (Table 1). Furthermore, the complexity of a controller meeting all the requirements must be feasible to implement, i.e. executed at a sampling rate that will not cause unacceptable discretisation errors as well as fast as possible so that it requires the minimum processing time, giving the opportunity to all the processes that must be executed to be carried out. If the grid conditions are such that the network operator demands them, then the clear choice would be the LCDRPLL. If, however, the grid is stiff and not vulnerable to disturbances such as the aforementioned, the ddsrfPLL could be the preferred choice because of its fastest response. In general, the PLL selection depends on the type of grid to which the PLL is connected, the dynamic response of the system

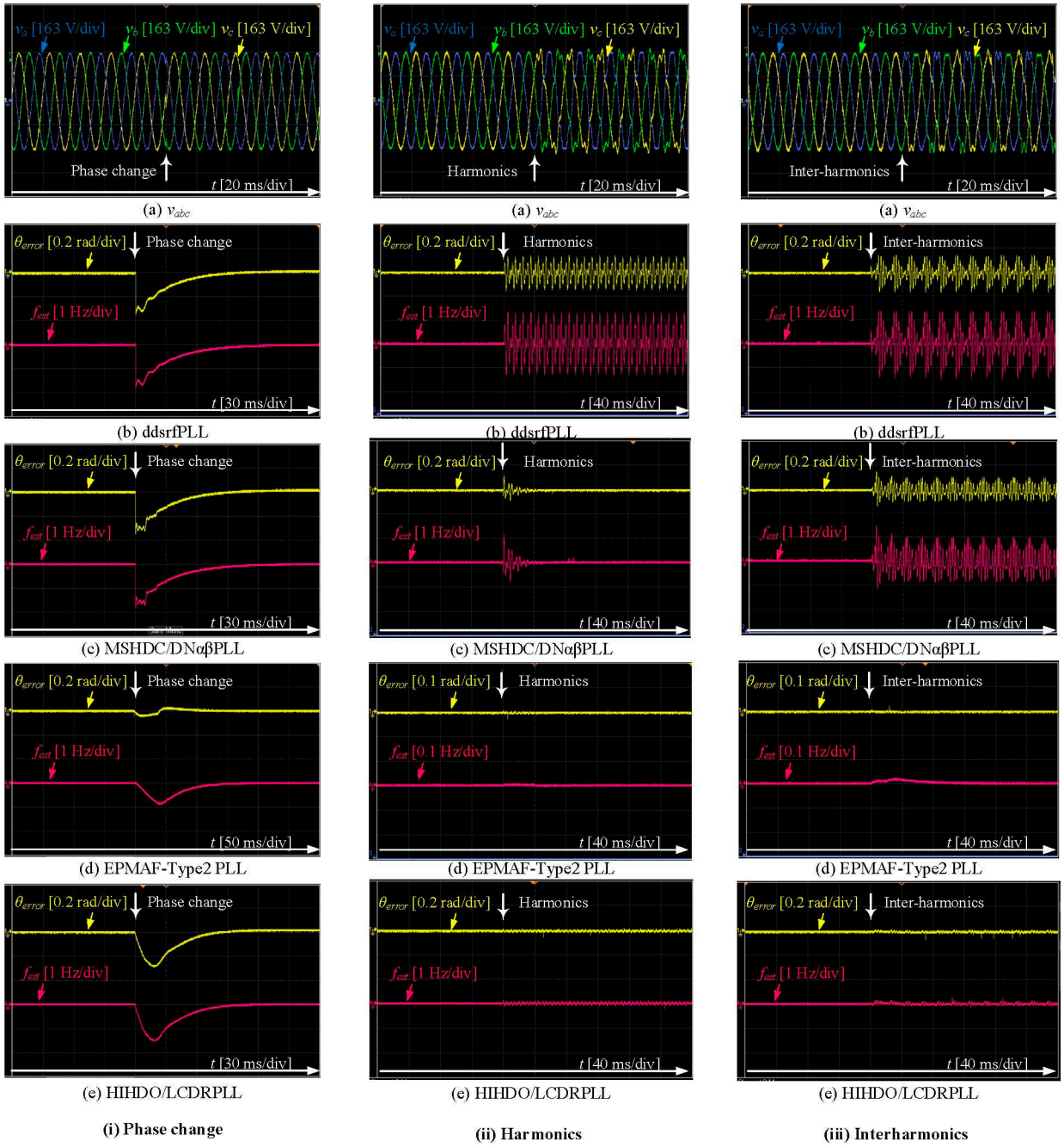

Fig. 17 *Experimental benchmarking of the PLLs*

(i) Under −20° phase change event

(a) v_{abc}, ***(b)*** ddsrfPLL, ***(c)*** MSHDC/DN*αβ*PLL, ***(d)*** EPMAF-Type2 PLL, ***(e)*** HIHDO/LCDRPLL

(ii) In the presence of harmonics

(a) v_{abc}, ***(b)*** ddsrfPLL, ***(c)*** MSHDC/DN*αβ*PLL, ***(d)*** EPMAF-Type2 PLL, ***(e)*** HIHDO/LCDRPLL

(iii) In the presence of interharmonics

(a) v_{abc}, ***(b)*** ddsrfPLL, ***(c)*** MSHDC/DN*αβ*PLL, ***(d)*** EPMAF-Type2 PLL, ***(e)*** HIHDO/LCDRPLL

and the computational complexity. Among the four PLLs investigated, the HIHDO/LCDRPLL is superior for applications, where all operations and a fast-dynamic response are required. The EPMAF type-2 PLL, however, is suitable for applications, where computational complexity is of major concern despite its high settling time (low dynamic response) that should perhaps be taken into consideration when making a decision. Concluding, there are three main pillars that one should consider when selecting a PLL (Table 1). The first is the capabilities that the PLL should be able to deal with something that is grid dependent and is a decision of the network operator. The second is the settling time, a characteristic that should be taken into consideration as it affects the dynamic response of the system. The third and as equally as important concerns the complexity and the physical implementation of the PLL. The sampling time should be as such so that no discretisation errors occur as these could, in the end, defeat the purpose. Since the sampling rate directly affects the processing time required by the microcontroller, particular care is necessary. The microcontroller does not only have to execute the PLL algorithm, but a range of other peripheral control processes, and to this end, every decision matters, especially if the resources of the microcontroller are limited. Even though microcontrollers are more advanced these days and capable of handling more processes, the expectation they should do more and run faster, may at end constitute this advancement an advantage with no net benefit.

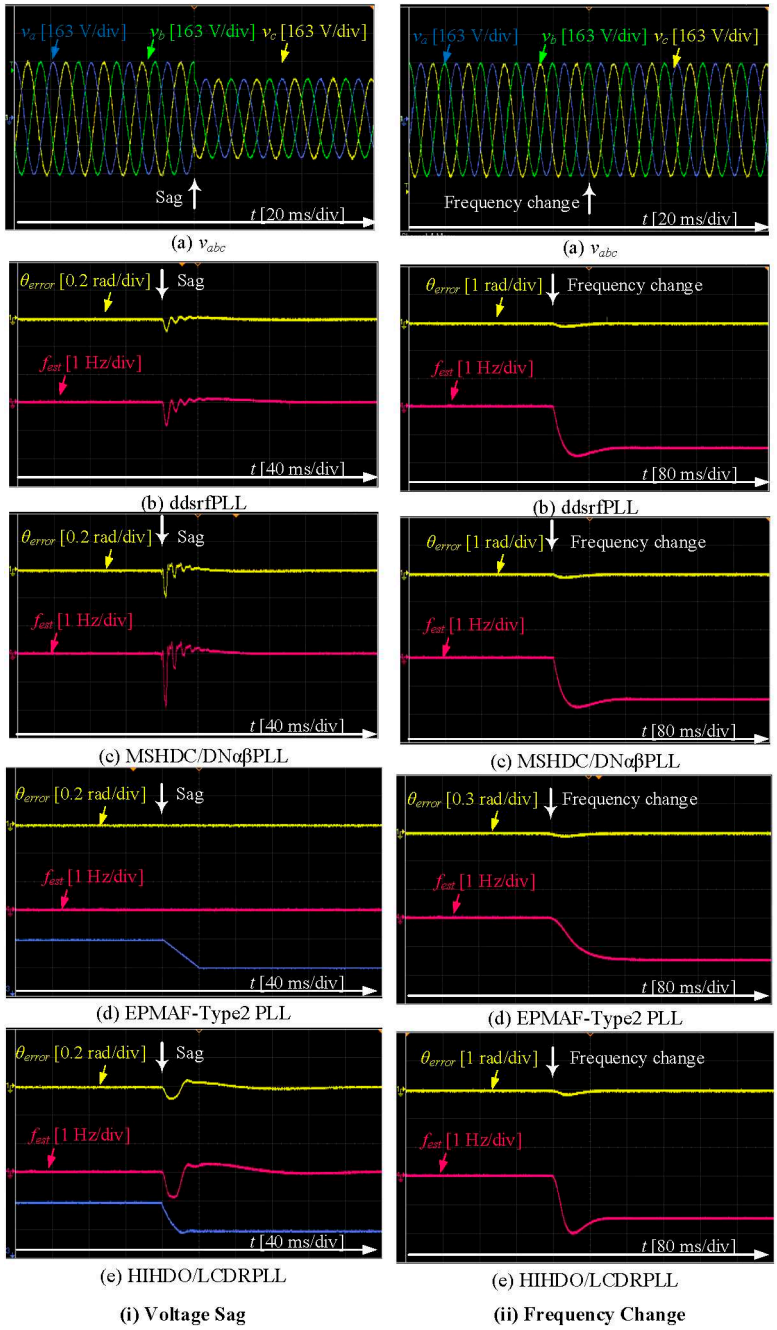

Fig. 18 *Experimental benchmarking of the PLLs*

(i) Under voltage sag event

(a) v_{abc}, ***(b)*** ddsrfPLL, ***(c)*** MSHDC/DN*αβ*PLL, ***(d)*** EPMAF-Type2 PLL, ***(e)*** HIHDO/LCDRPLL

(ii) Under frequency change

(a) v_{abc}, ***(b)*** ddsrfPLL, ***(c)*** MSHDC/DN*αβ*PLL, ***(d)*** EPMAF-Type2 PLL, ***(e)*** HIHDO/LCDRPLL

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