ENHANCED PERFORMANCE BIDIRECTIONAL QUASI-Z-SOURCE INVERTER CONTROLLER

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Abstract

A novel direct control of high performance bidirectional quasi-Z-source inverter (HPB-QZSI), with optimized controllable shoot-through insertion, to improve the voltage gain, efficiency and to reduce total harmonic distortion is investigated.

The main drawback of the conventional control techniques for direct current to alternating current (DC-AC) conversion is drawn from the multistage energy conversion structure, which implies complicated control, protection algorithms and reduced reliability due to the increased number of switching devices.

Theoretically, the original Z-source, Quasi-Z-source, and embedded Z-source all have unlimited voltage gain. Practically, however, a high voltage gain (>2 or 3), will result in a high voltage stress imposed on the switches.

Every additional shoot-through state increases the commutation time of the semiconductor switches, thereby increasing the switching losses in the system. Hence, minimization of the commutation time by optimal placing of the shoot-through state in the switching time period is necessary to reduce the switching loss. To overcome this problem, a combination of high performance bidirectional quasi-Z-source inverter with a sawtooth carrier based sinusoidal pulse width modulation (SPWM) in simple operation condition for maximum boost control with 3rd harmonic injection is proposed. This is achieved by voltage-fed quasi-Z-source inverter with continuous input current, implemented at the converter input side which

can boost the input voltage by utilizing the extra switching state with the help of shoot-through state insertion technique.

This thesis presents novel control concepts for such a structure, focusing mainly on the control of a shoot-through insertion. The work considers the derivation and application of direct controllers for this application and scrutinizes the technical advantages and potential application issues of these methodologies.

Based on the circuit analysis, a small signal model of the HPB-QZSI is derived, which indicates that the circuit is prone to oscillate when there is disturbance on the direct current (DC) input voltage. Therefore, a closed-loop control of shoot-through duty cycle is designed to obtain the desired DC bus voltage. The DC-link boost control and alternating current (AC) side output control are presented to reduce the impacts of disturbances on loads.

The proposed strategy gives a significantly high voltage gain compared to the conventional pulse width modulation (PWM) techniques, since all the zero states are converted into shoot-through states. The simulated results verify the validity and superiority of the proposed control strategies.

Acknowledgement

This project is by far the most significant accomplishment in my life. Various people deserve my sincere thanks for their immeasurable help to me throughout the course of this thesis. I would like to express my gratitude to my research advisors being Dr Wada Hosny from department of Architecture, Computing and Engineering (ACE) for his intensive supervision, guidance and trust through my candidature at University of East London. His door was always open for all students during his time at University of East London and his energy and enthusiasm in research has been a major source of motivation.

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Dedication

I would like to dedicate this Doctoral dissertation to my lovely parents and my kind and beautiful wife. There is no doubt in my mind that without their constant loves, endless support and encouragements I could not have completed process.

سپاس و ستایش خدای جل و جلاله را که آثار قدرت او بر چهره روز روشن، تابان است و انوار حکمت او در دل شب تار، درفشان. آفریدگاری که خویشتن را به ما شناساند و درهای علم را بر ما گشود و عمری و فرصتی عطا فرمود تا بدان، بنده ضعیف خویش را در طریق علم و معرفت بیازماید.

این مجموعه را تقدیم می کنم به:

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به پاس تعبیر عظیم و انسانی شان از کلمه ایثار و به پاس عاطفه سرشار و گرمای امیدبخش وجودشان که در این سردترین روزگاران بهترین پشتیبان است و به پاس قلبهای بزرگشان که فریادرس است و سرگردانی و ترس در پناهشان به شجاعت می گراید و به پاس محبت های بی دریغشان که هرگز فروکش نمی کند.

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Abbreviations

A	Ampere
AC	Alternating Current
AC-AC	Alternating current-Alternating current
AC-DC	Alternating current-Direct current
B	Boost factor
C	Capacitor
CSI	Current Source Inverter
CCM	Continuous Conduction Mode
D	Diode
DC	Direct Current
DC-AC	Direct Current-Alternating current
DC-DC	Direct current-Direct current
DG	Distributed Generation
Ds	Shoot through duty ratio
EMI	Electromagnetic Interference
HPB-QZS	High Performance Bidirectional Quasi-Z-Source
HPB-QZSI	High Performance Bidirectional Quasi-Z-Source Inverter
Hz	Hertz
IGBT	Insulated-Gate Bipolar Transistor
KVar	KiloVar
kW	Kilowatt
LC	Inductor-Capacitor
MI	Modulation Index
MPPT	Maximum Power Point Tracking
MSVM	Multilevel Space Vector Modulation
nF	Nano Farad
NPC	Neutral Point Clamped
NTV	Nearest Three Vector

P	Proportional
pF	Pico Farad
PI	Proportional-Integrator
PID	Proportional-Integral-Derivative
PSM	Phase Shift Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
QZSI	Quasi-Z-Source Inverter
RCM	Reduced Common Mode
RES	Renewable Energy Systems
SBI	Switched Boost Inverter
SPWM	Sinusoidal Pulse Width Modulation
SSA	Small Signal Averaging
STC-PWM	Sawtooth Carrier-Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
TSTS	Three-Switch Three-State
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter
ZVS	Zero Voltage Switching

Chapter 1

Introduction

The past decade has witnessed significant development in power conversion technology, thanks to the continuous penetration of power electronics into power generation, transmission and consumption. Power generated from renewable resources is either connected to the grid or to the local loads through inverters. With the performance improvement and cost reduction of the power electronics devices, new topologies of the power converters have become available, reducing the size, saving the energy, and improving the efficiency of the system. The successful operation of the direct control of high performance bidirectional quasi-Z-source inverter (HPB-QZSI) with controllable shoot through insertion requires the knowledge of power electronics, converter operation, switching scheme and most important of all control loop design. The focus of this thesis is on reducing total harmonic distortion and improving voltage gain. The simplification of the available switching scheme and proposed shoot through insertion technique are also considered. A control loop is designed based on a real-time system so that the whole system can meet the design specifications.

1.1 Converters classification

Power converters control the flow of power between two systems by changing the character of electrical energy: from direct current to alternating current, from one voltage level to another voltage, or in some other way.

Here, some important way to classify the power converters are described. The aim of this section is not to make a rigorous converter classification, neither to make a state of the art, because it is not the purpose of this thesis. It is only desired to understand some properties of these kind of circuits.

The most common classification of power conversion systems is based on the waveform of the input and output signals, in this case whether they are alternating current (AC) or direct current (DC) (Christiansen, 1996), thus:

• DC to DC converter (Chopper).

• DC to AC converter (Inverter)

• AC to DC converter (Rectifier)

• AC to AC converter (Transformer)

At the same time, the devices within converters can be switched in different ways (Alexander Kusko, 2007). If the devices switch at the line frequency (normally, 50Hz or 60Hz), they can be line frequency converters (naturally commutated converters) or high-frequency switching (forced-commutated converters). Depending on the character of the input source, they may be voltage-source converters or current-source

converters. Moreover, converters may be of low, medium or high voltage and/or current level. Another sort of classification may be performed according to the size of the output signal obtained from the input signal; if the converter accomplishes a lower output signal it is well known as step-down, and if it obtains a larger signal, it is known as step-up(Acha, 1997).

1.2 Research Motivation

Impedance-source networks provide an efficient means of power conversion from/to a source or load in a wide spectrum of electric power conversion (DC-DC, DC-AC, AC-DC, and AC-AC) applications (Peng, 2002; Fang Zheng, 2003). Since the publication of the first impedance-source network called a “Z-Source Network” in 2002, many modified and new impedance network topologies have been reported in the literature with both buck and boost capabilities. The total number of publications in the relevant fields has exceeded one thousand and opened a new horizon in the field of power electronics and drives.

All electric power conversion topologies inspired from impedance network with reorganizing LC components (Anderson and Peng, 2008; Shuai and Peng, 2011) . The quasi impedance source network is a modified topology derived from the Z-source topology, employing an impedance network which couples the source and the inverter to achieve voltage boost and inversion (Peng, 2003).There is no one size topology to apply in all applications. Each topology has different modification and control techniques according to their own unique properties.

Renewable energy generation, such as PV, wind power, and motor drives are prospective applications of quasi-Z-source converters because of the unique voltage buck–boost ability with minimum component count and potential low cost. In addition to small passive components (inductor, resistor or capacitor), high performance and power density, the new power electronic devices have high switching frequency and less loss. Quasi-Z-source converters still can be used as advance topologies for various applications.

Modifying the quasi-Z-Source circuit can produce distinct trait for various application needs. New quasi-Z-source topologies are still being developed, mainly for four reasons:

- To reduce the quasi-Z-source network component count and rating.
- Extension of voltage gain range.
- Achieving higher power density.
- Application-oriented optimization and improvement.

However, the traditional QZSI only allows unidirectional power flow from the DC to the AC side. To achieve the bidirectional power flow capability, the same approach as in (Anderson and Peng, 2008; Zakis et al., 2011) is utilized in this thesis and the diode in the quasi-Z-source network (QZSN) is replaced by an active switch (S7) [See Figure (4.2)], and additional small capacitor to enhance the performance of the system. A similar approach is also utilized in the bidirectional ZSI in (Haiping et al., 2008; Rabkowski et al., 2008). The analysis proves that with the active switch, the

inductor currents in the quasi-Z-source network can be reversed and the energy from the ac side can be delivered to the DC source. The analysis also shows that, unlike in the ZSI, part of the DC-link ripple current will be absorbed by the two capacitors in the quasi-Z-source network and not go through the DC source [see Figure. (2.10 b)]. Furthermore, with the additional switch, the discontinuous conduction mode (DCM) can be avoided and the bidirectional quasi-Z-source inverter (BQ-ZSI) can have a better performance with small inductance or under low power factor condition (Miaosen and Fang Zheng, 2008b), such as when the electric motor is operated with a light load.

In the new proposed system, an appropriate combinations of HPB-QZSI with various topologies makes an extensive range of electric power conversion topologies from a medium range of voltage and current to a high range of voltage and current. Furthermore, all switching configuration such as unidirectional/bidirectional and isolated/non-isolated can be used and applied for all kind of inverters to fulfil the various electric power application's requirements.

1.2.1 Control methods

To have a desirable output voltage and output current along with amplitude, frequency and phase, various control methods and modulation techniques are indispensable to control and modulate the converters. Moreover, all control techniques and pulse width modulation by modifying the shoot-through zero state to control the high performance bidirectional quasi-Z-Source converter are still valid. However, in addition to all states

in the traditional modulation techniques, a new state called a “shoot-through state” is introduced and embedded into the modulation strategy without violating the volt-sec balance in the operating principle. New pulse width modulation technique is inspired from sinusoidal PWM; utilizing the distinctive properties of shoot-through state are advanced to obtain the maximum DC-link voltage.

In this control strategies by modifying the shoot-through state ($\mathrm{D_{st}}$) can control the voltage of the capacitor, also with modifying modulation index can control the output voltage, utilizing distinct P/PI controller. Different closed loop control techniques can be seen in literature to control the DC-link voltage and improve the transient response of quasi-Z-source inverter which inspired from the effect of varying parameter, poles and right half plane zeroes. All control techniques have two control degrees of freedom i.e. shoot-through time period ($\mathrm{D_{st}}$) to control the DC-link directly/indirectly; and modulation index (M) to control the output voltage. The best modulation techniques to maximize the boost, minimize the harmonic distortion, reduce the switches stress and reduce the number of device commutations in each switching period can be achieved by amalgamation of conventional switching concept along with selective shoot-through zero state.

1.2.2 Modulation techniques

Different pulse width modulation methods with the purpose of reducing the commutation times, less voltage stress and easy implementation are discussed in the literature. various modification including simple boost, maximum boost and maximum

constant boost as well as constant boost with 3rd harmonic injection are presented in (Fang Zheng et al., 2005b; Yuan et al., 2009). The simple boost inspired from the conventional SPWM. Comparing the triangular signal with reference signal provides the sinusoidal signal and two straight lines to generate the shoot through time period for boosting the output voltage. By 3rd harmonic injection can increase the range of modulation index from 1 to $2/\sqrt{3}$, also by utilizing two straight lines ($V_{P,}$ V_n) can produce the shoot through state.

In the simple maximum-boost control, the modulation index is limited to M= 0.5 which means that the maximum voltage gain can only go up to 0.944. Maximum boost control utilizes all the zero states as shoot-through states. The range of modulation index is extended to 0.866 by injecting the third harmonic signal in the reference signal. In terms of the total harmonic distortion (THD) at the output, the maximum constant boost control method is effective in eliminating low order harmonics compared to the simple boost and maximum boost controls. A comparison of various control methods is also presented in (Qin et al., 2011a).

1.2.3 Boost inverter

Quasi-Z-source inverters are adapted as power conditioning circuits because they combine the functions of voltage boost and DC-AC conversion. The conventional voltage source inverter (VSI) and current source inverter (CSI) suffer from the limitation of triggering two switches in the same leg or phase and in addition, the maximum obtainable output voltage cannot exceed the DC input. Both Z-source

inverters and quasi-Z-source inverters overcome these drawbacks; by utilizing several shoot-through zero states, in which two switches in the same leg are fired simultaneously to boost the output voltage (Joel Anderson, 2008). Sustaining the six permissible active switching states of a VSI, the zero states can be partially or completely replaced by the shoot through states depending upon the voltage boost requirement. High performance bidirectional Quasi-Z-source acquire all the advantages of traditional Quasi-Z-source inverter. The HPB-QZSI extends several advantages over the QZSI such as:

- Reduction in voltage stress across the quasi-Z-network capacitor by keeping the modulation index high.
- Voltage source and inverter bridge share the same ground point which leads to low leakage current.
- Reduced inrush current during start-up because of the front capacitor, hence the ripple current in inductor is filtered out.
- Wide range of load operation even with a small inductance in the HPB-QZS network.

These advantages make the HPB-QZSIs suitable for power conditioning in renewable energy systems (RES) like fuel cells, photovoltaic cells, motor drive, etc.

1.2.4 Total harmonic distortion reduction

The output voltage of PWM power inverters shows harmonic distortion due to several causes; the main ones are modulation algorithm, nonlinearities in the output filter,

dead times, voltage drops across the switches and modulation of the DC bus voltage (A. Oliva, 2005). With the use of non-linear loads on the rise globally, isolation for poor quality distribution system and mitigation of harmonics will become increasingly important. The limit per IEEE Std 519 are not enforced limits but suggestion on acceptable levels. As a result, THD on certain power system could be much higher, especially considering the difficulty in attaining harmonic measurements.

1.3 Main Objectives

Power converters provide a crucial function in renewable energy by converting power from renewable sources to match the voltage, frequency and other requirements of the system. The aim of the research is to improve the voltage gain and reduce the total harmonic distortion of the power converter. The research objectives can be broadly classified as:

(I) Investigate various techniques for good estimation of the converter topology characteristics, such as efficiency, reliability, transmission, distribution and delivery

(II) Development of accurate models for various topologies and perform comparison analysis

(III) Investigate feasibility of high frequency modulation techniques for reducing switching losses.

(IV) Satisfactory power quality of the output voltage or current, commonly known as desired magnitude, frequency and limited THD content; sufficient voltage

boost for desired AC voltage level in case that the output voltage level is adequate.

(V) Development of a new control technique along with controller for effective shoot-through insertion and verify the results using Simulink software.

(VI) Development of a design tool-box in Matlab/Simulink implementing the design control system.

1.3.1 Research Aims to Investigate

The research questions will be addressed on following specific objectives to fulfil the overall objectives.

- Can the new control technique regulate the required voltage despite variations in output voltage of renewable sources?
- What is the effect of using small inductors on ripple and THD?
- What is the maximum efficiency achievable on the new proposed strategy?
- Can the same method be applied for high power applications?
- Can the simulations results be optimized for the method proposed?

There is no complete systematic study for above questions due to the complexities and uncertainties involved in the proposed converter control technique. It is thus appropriate that with such different channel techniques a number of case studies are to be carried out so as to provide guidelines for a possible future optimal planning and design of the power electronic converter topology.

1.3.2 Problem scope

Analysis of the converter topologies studied earlier shows that they are not well suited for renewable energy applications due to high level of designing complexity in the DC-AC inverter. According to the literature review of the related work, the new proposed converter control technique is an alternative for existing high frequency converter topology. Effective control techniques for each component including the capacitors and inductors are required.

The control technique proposed, offers good input voltage boost properties and relatively simple power circuit. Even so extensive simulations of the proposed techniques are to be performed to verify its ability to ensure necessary output voltage at all defined operation modes. Although, a top down approach was identified as a best available technique for reducing harmonic distortion caused by number of branches and loads [See Figure (6.8)]; likewise switching losses also need to be considered by using high frequency modulation ratio.

1.4 Contribution to knowledge

The proposed high performance bidirectional quasi-z-source and sawtooth carrier based SPWM in simple operation condition for maximum boost direct control with common mode (3rd harmonic) injection has uniformly spaced shoot-through states, promising a high output voltage gain and reduced THD, with less voltage stress on the bridge compared to triangular carrier PWM. The control method presented has good voltage regulation capabilities at a relatively simple power circuit. In addition, the

switches achieve zero voltage switching (ZVS) which reduce EMI and improves efficiency of the inverter.

The novel areas of this research are:

- Development of a new control technique for quasi impedance source converter topologies for Low/Medium power applications.
- Investigation of a novel control technique of the converter topology which converts variable voltage level and frequency expected from a renewable energy to a voltage level and frequency which could be interfaced with the grid.
- Development of a new accurate control technique for DC-AC converter to reduce the switching losses as only one of the phase leg is gated during shoot through states.
- Development of new technique to involve alternative active state and shoot through state and no zero state. Hence, it reduces the ripple content in inductor current.
- Investigation on voltage stress across the switches to keep the modulation index high and reduce the voltage stress.
- Development of a technique to enhance the fundamental voltage by reducing the THD.

This section outlines areas of work that have not been published before or not covered in details in the current literature.

1.5 Thesis Overview

A brief description of each chapter is provided below:

1.5.1 Chapter 1

Provides a general introduction covering recent developments in power electronics technology and how they play an important role in terms of control of a three-leg VSI. The motivations and objectives of the research are introduced, methodology of the project is presented, and the thesis overview is also covered.

1.5.2 Chapter 2

Provides a comprehensive investigation on the topic of impedance source network based power converters/inverters and is organized as follows: first section categorizes the available impedance-source power converters/inverters based on conversion functionality and further subcategorizes them into different switching configuration. Second section describes different impedance-source network topologies segregated as transformer/ coupled inductor or no transformer. Finally, provides a comparison of different impedance network-based converters and a conclusion.

1.5.3 Chapter 3

Elaborates different control techniques to apply for different applications, also considering the most applicable control methods and modulation techniques for impedance source network and evaluation of the system based on performance and complexity. A comprehensive investigation on operation principal, modelling and

control and is organized as follow: first section classifying general modulation techniques. Second section describes the operation modes and characteristics of quasi-z-source with small inductance. Last section is investigate on the harmonic distortion and its effect in electrical power systems.

1.5.4 Chapter 4

Analyses the mathematical model of an enhanced quasi-z-source network and an in-depth performance analysis for different switching schemes on enhanced quasi-z-source using the sawtooth carrier method with 3rd harmonic injection method is presented. Voltage harmonic factor, inductor current harmonic factor, conduction losses and switching losses of different switching schemes are compared. The analysis describes a design of the system control based on the model in continues time domain. Simplified switching scheme named controllable shoot through insertion PWM is also introduced.

1.5.5 Chapter 5

Design of the DC side and AC side controller along with direct control to sense and measure the peak-DC-link voltage with PI controller guarantees the performance of the system under steady state and transient state conditions.

1.5.6 Chapter 6

Illustrates simulations and validation of the result, using the combination of Matlab/Simulink and Matlab/Simpower. Further, discussion of output harmonic spectra

of various output voltages and currents, also total harmonic distortion measurement for each output.

1.5.7 Chapter 7

Summarizes the thesis with conclusions and recommendations for future research.

Chapter 2

Literature review (Electric power Conversion System)

2.1 Overview

In electric power conversion applications such as (DC–DC Converter, DC–AC Inverter, AC–DC Rectifier, AC– AC Converter), impedance network deliver an effective meaning of power conversion among source and load (Peng, 2002;Fang Zheng, 2003). The literature presents different topologies and control techniques with different type of impedance network, e.g., Z-source inverter system and control for adjustable speed drives (Peng et al., 2003; Fang Zheng et al., 2005a), Distributed Generation Applications (photovoltaic applications, Wind, Fuel cell, etc.), (Yuan et al., 2013; Gajanayake et al., 2007).

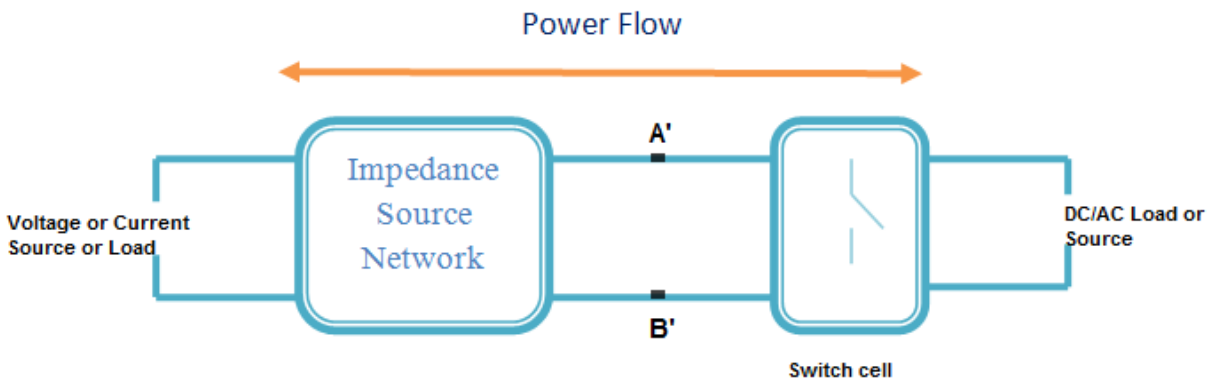


Figure 2.1 General circuit configuration of impedance-source network for power conversion with different switching cells

Appropriate implementation of the impedance networks with different switching configuration, topologies and different switching devices makes a possibility of various power converter topologies with buck, boost, buck-boost, unidirectional, bidirectional, isolated and also non-isolated converter (Siwakoti and Town, 2014; Xu Peng et al., 2011). Possible switching structures with general configuration depend on the requirement of different application for power conversion systems shown in Figure (2.1). The simple impedance network normally is an amalgamation of basic linear elements i.e., Inductor (L) and Capacitor (C). Components like Resistor (R) which is dissipative, are normally avoided. However, enhancing the performance of the system with different configuration is achievable by adding a nonlinear element e.g., switches, diodes and combination of both to the impedance source networks. Electric power conversion systems, voltage source inverter (VSI) and current source inverter (CSI), have some limitation; to overcome this limitation, the impedance source network have invented (Peng, 2002; Zhi Jian et al., 2008). Voltage source inverter act as a buck inverter; hence, the ac output voltage is less than input voltage which is not enough for ac drives alone and to feed the need of distributed generation (DG). To achieve required AC output voltage, having a DC-DC converter is necessary, but the cost of the system due to additional component will increase which is the cause of reducing the efficiency. In addition, short circuiting across the inverter bridge because of misgating-ON, will destroy the switches as the electromagnetic interference (EMI) has a negative impact on switching devices. Having distortion waveform at the output is because of dead time presentation in such cases. On the other hand, the output

voltage in current source inverter is more than input voltage, therefore, for an application which requires a wide range of voltage is compulsory to have an additional DC-DC buck converter.

Further, in this case, the upper and lower leg of the switches have to be gated-ON and preserved to prevent an open circuit which will destroy the switching devices. Various switching configuration for different application are utilizing the impedance networks attributes with various pulse width modulation and control techniques. Possible switch configuration range from simple-single switch topologies to very complex controlled multilevel and matrix configuration presented in (Fang Zheng et al., 2005b; Miaosen and Fang Zheng, 2008b).To overcome the limitation and conceptual barriers of traditional voltage source (VSI) and current source inverter (CSI), the impedance source converter provides a new electric power conversion concept. Impedance source network can operate as a voltage source inverter (VSI) or current source inverter depending on different applications; also, output voltage can vary between (0 - ∞).

The first impedance source network called “Z-source network” published in 2002 (Peng, 2002), since then different altered topology with enhanced modulation and control techniques for different applications have been published (Fang Zheng, 2003; Liming et al., 2011). The simple Z-source network shown in Figure (2.2) includes of inductors (L1, L2) and Capacitors (C1, C2) connected as a Z shape which can be voltage or current source as a buffer between source and load.

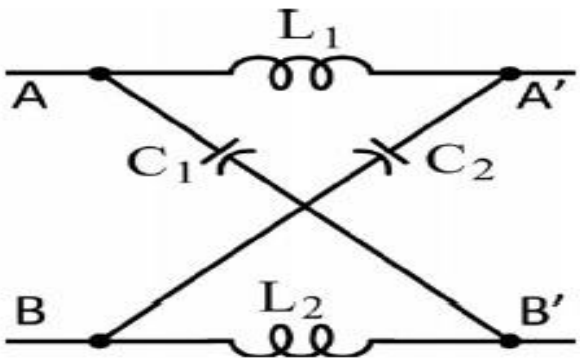


Figure 2.2 Basic Z-Source impedance network

2.1.1 Operating Principle of the Impedance-Source Converter

The impedance source can be used for any (AC-AC), (AC-DC), (DC-DC) and (DC-AC) conversion system. The Z-source is an example of demonstration of the principal operation and control of the impedance-source-network. Figure. (2.3) shows the circuit diagram of the Z-source converter and its equivalent circuit during active and shoot-through states. Output terminals are short circuited in the period of shoot-through state with conduction of switches, which causes reversing the bias in the circuit with diode D.

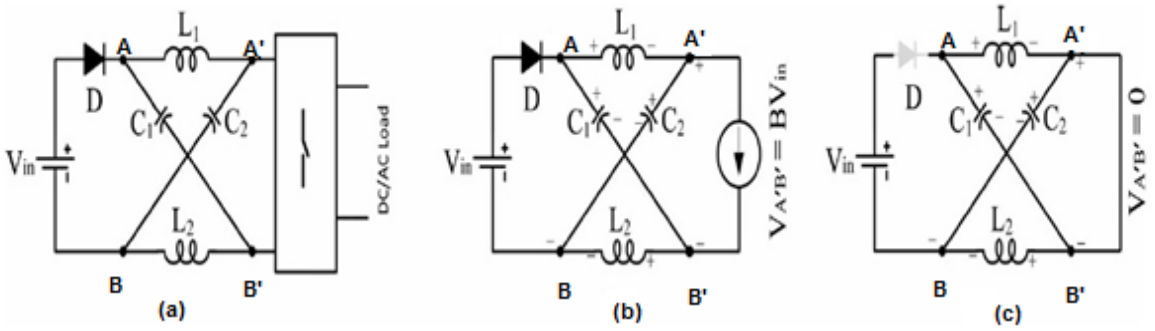


Figure 2.3 (a) Voltage-fed Z-source converter illustrating its equivalent circuit during (b) active state and (c) shoot-through state

In the period of active state the diode D will conduct and also the energy which is stored in passive component (Capacitor, Inductor) in the shoot-through state time will transfer to the load. The switching circuit viewed from the DC side during the active state is equivalent to a current source as shown in Figure. (2.3(b)). Averaging of these two switching states results in an expression to compute the peak DC-link voltage,$(\hat{v})_{A'B'}$ across terminals A′ and B′, in terms of its input voltage V_{in} as:

$$(\hat{\mathrm{v}})\,\mathrm{A}',\mathrm{B}' \;=\; 1/(1-\beta \mathrm{D}_{\mathrm{st}})\,\mathrm{V}_{\mathrm{in}} \;=\; \mathrm{B}\,\mathrm{V}_{\mathrm{in}} \qquad (2.1)$$

Where D_{ST} is the fractional shoot-through time assumed in a switching period, B is boost factor and β ≥ 2 is a factor determined by the impedance network chosen, e.g., for Z-source inverter and quasi-Z-source inverter (ZSI and QZSI), $\beta = 2$.

Equating the denominator of the boost factor (B) to zero, then results in the permissible range of D_{ST} as $0 \le D_{st} < \frac{1}{\beta}$, whose upper limit corresponds to an infinite gain.

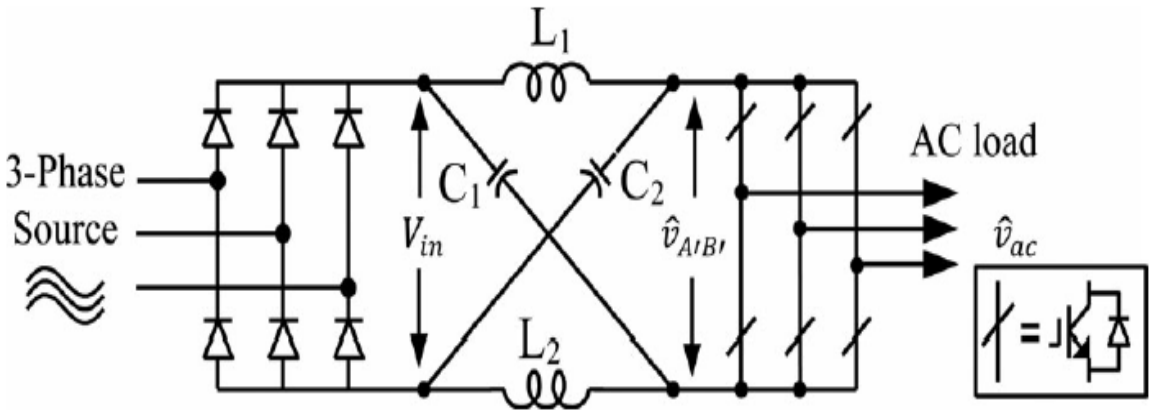


Figure 2.4 Voltage-fed ZSI—an example of a ZSI

Figure (2.4) shows a three-phase voltage fed Z-source inverter which demonstrates the principal operation of Z-source inverter. The advantage of Z-source inverter in

comparison to traditional three-phase voltage source inverter is in switching state, which ZSI has 9 permissible switching states that includes six active states, two zero states and one shoot through state; whereas, the traditional VSI has eight switching states, six active states and two zero states (No shoot through state). In the period of zero state, three upper/lower legs are gated ON simultaneously which is the cause of having short circuit in output terminal and generating zero voltage across the load (Peng, 2002). Similarly, in shoot-through state also, the voltage across the load is zero; but, the output voltage can be boosted simultaneously. The basic voltage source inverter has no shoot-through state as it would destroy the circuit by short circuiting across the DC-link. The Z-source network and the shoot-through zero state provides a unique buck–boost capability for the inverter by varying the shoot-through time period and modulation index (MI) of the inverter.

According to (2.2) ideally, the output voltage can be change between 0 to ∞).

$$v\hat{}ac = \frac{MB}{2}Vin = \mathrm{M}\,[1 - 2\mathrm{Dst}]^{-1}\frac{V_{in}}{2} \qquad (2.2)$$

To prevent surpassing device limitation, some practical features and converter's performances are essential to be considered for high voltage buck/boost manoeuvres. The impedance source network converters can be controlled by all traditional pulse width modulation techniques. As discussed earlier "shoot-through state" is the new state in electric power conversion which introduce to modulating techniques with reverent to the volt-sec balance in any operation principles. Shoot-through state has an inimitable trait that many new pulse width modulation methods from sinusoidal and

SVPWMs (Fang Zheng et al., 2005b; Miaosen and Fang Zheng, 2008b) are produced to regulate the output voltage. In addition, there are various control methods applied for various applications which will be discussed in detail.

2.1.2 Status of impedance source topologies and applications

First proposal for impedance network called Z-source inverter was in 2002 which developed swiftly; various topologies for Z-source and different modification have developed exponentially.

Electric power converters can be segregated in four categories .i.e., converter (DC-DC), Inverter (DC-AC), Transformer (AC-AC), Rectifier (AC-DC). A further breakdown leads to two-level and multilevel (Asano et al., 2011; Banaei et al., 2012), AC–AC and matrix converters (Husev et al., 2012; Minh-Khai et al., 2010), and non-isolated and isolated DC–DC converters (Siwakoti and Town, 2014; Honnyong et al., 2010). From the Z-source network topology standpoint, it can be Voltage-fed or Current-fed. Further, impedance network can be divided based on the magnetic used in the impedance source network, i.e., non-transformer based (Qin et al., 2009b; Gajanayake et al., 2010), and transformer or coupled inductor based (Gajanayake et al., 2009; Shuai et al., 2011).

The notion of impedance network has opened a new area of study in electric power conversion system. There is no one size impedance source topology to apply in all applications. Each topology has different modification and control techniques according to their own unique properties. Renewable energy generation, such as PV,

Wind Power, and Motor Drives are prospective applications of QZ/Z-source converters, because of the unique voltage buck–boost ability with minimum component count and potential low cost. In addition to small passive components (inductor, resistor, transformer, or capacitor), high performance and power density, the new power electronic device has high switching frequency, less losses, and high temperature capability.

2.2 Categories of impedance source converter based on conversion functionality

A comprehensive classification of impedance source power converters with various switching configuration are shown in Figure (2.5).

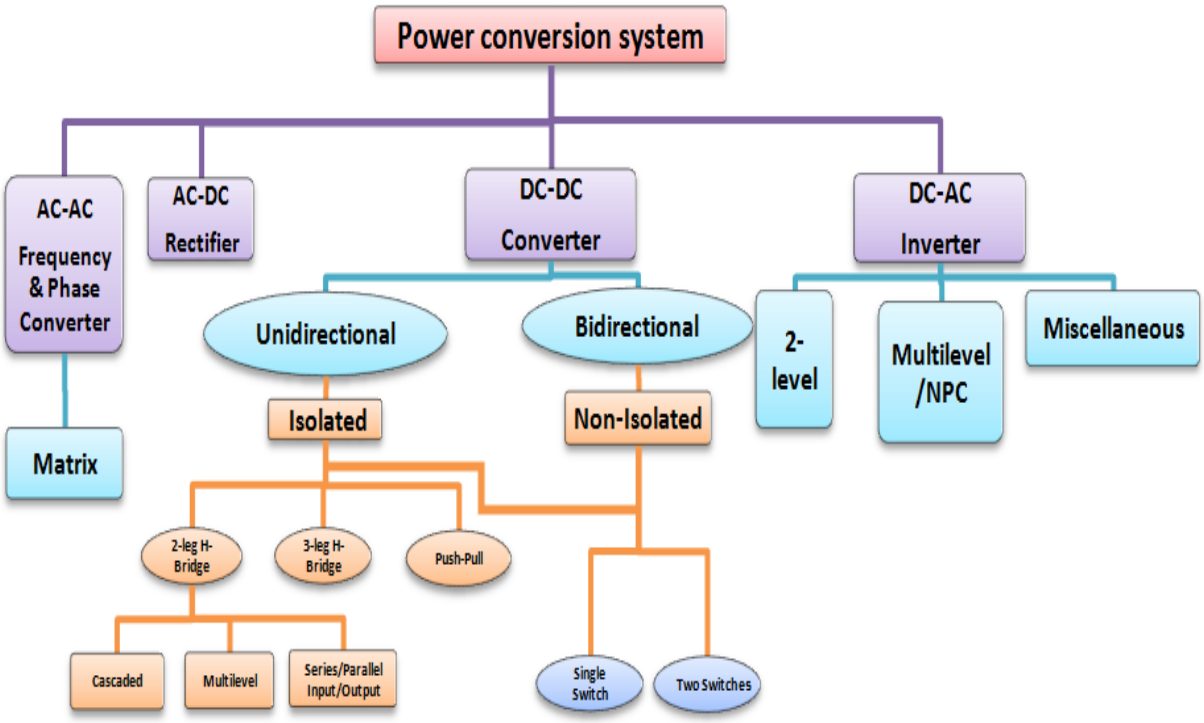


Figure 2.5 Categorization of impedance-source network-based power converters

However, the focus of this thesis is on DC-AC conversion system. Possible switching configuration for converters using multiple diodes and switches in unidirectional and/or bidirectional configuration for Z-source impedance are shown in Figure (2.6). Appropriate combination of impedance network with various topologies, makes an extensive range of electric power conversion topologies from medium range of voltage and power to high range of voltage and power.

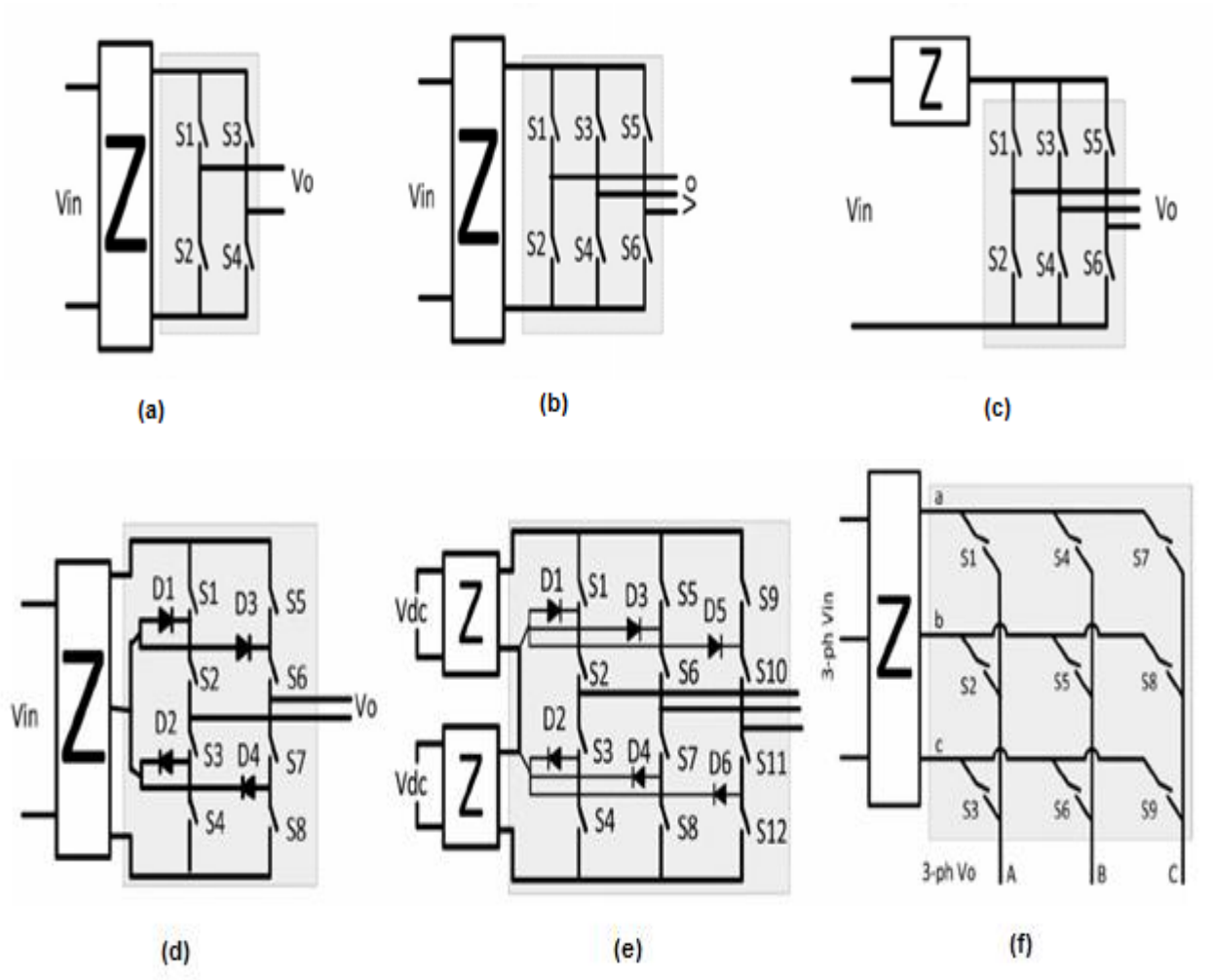


Figure 2.6 Possible switching configuration for converter; (a)-(f) using multiple diodes and switches (in unidirectional and/or bidirectional configuration) for DC-DC, DC-AC, AC–DC, and AC-AC converter (Z → impedance-source network)

Furthermore, all switching configuration (unidirectional/bidirectional, isolated/non-isolated) can be used and applied for all kind of converters, inverters, and rectifier to fulfil the various electric power application's requirements.

2.2.1 DC–DC Converter Topologies

The literature provides various modulation and different control techniques with different DC-DC converters (isolated/non-isolated). For example, a DC-DC converter realised using a QZSI with two or three-leg H-bridge switching topology is proposed for distributed generation (Vinnikov and Roasto, 2011; Siwakoti and Town, 2014)as shown in Figure. (2.7(a)). A new quasi-Z-source push–pull converter topology with a reduced number of switching devices is also proposed in (Siwakoti et al., 2014a)as shown in Figure. (2.7(b)).

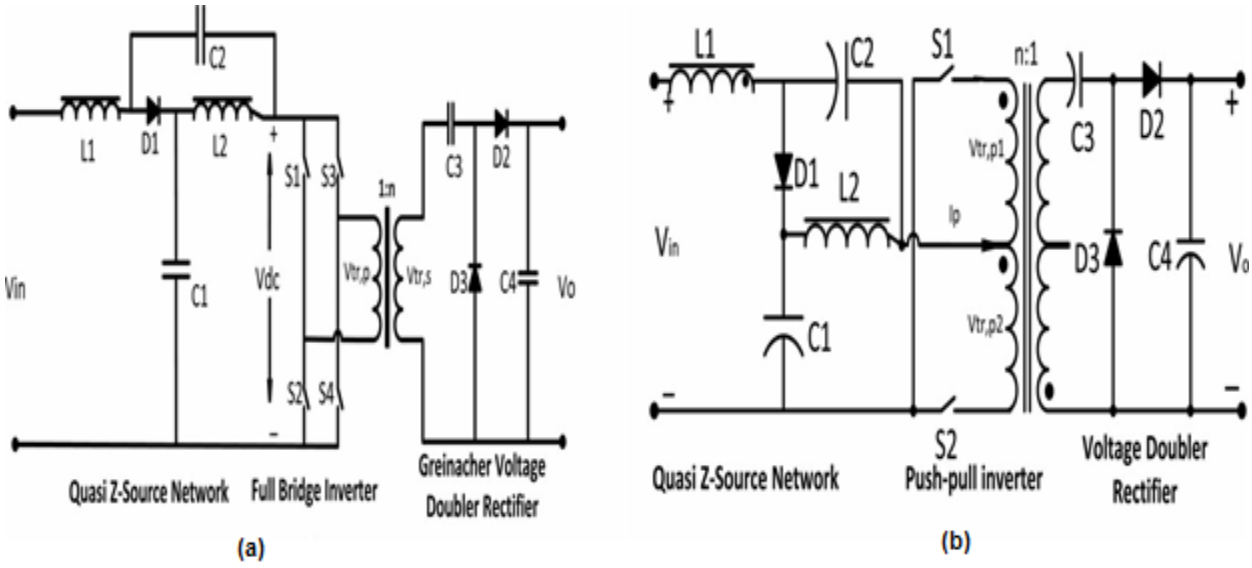


Figure 2.7 qZSI-based-isolated DC–DC converter with (a) intermediate H-bridge switching topology and (b) push–pull topology

It has the same gain as $2n/(3-4D_t)$, where $0.5 \leq D_t \leq 0.75$ as in (Siwakoti and Town, 2014; Vinnikov and Roasto, 2011); however, the complexity of gate circuit design is reduced.

A DC-DC converter with a trans-Z-source network is implemented in (Nguyen et al., 2013) as shown in Figure (2.8), with the aim of achieving higher boost at a lower shoot-through time period of the switch. Proper implementation could reduce the turn's ratio of the transformer as compared to other QZSI-based topologies. This advantage is utilized to design the converter to operate in parallel (Hyeongmin et al., 2012) to achieve higher power level and premium power quality along with improved system efficiency.

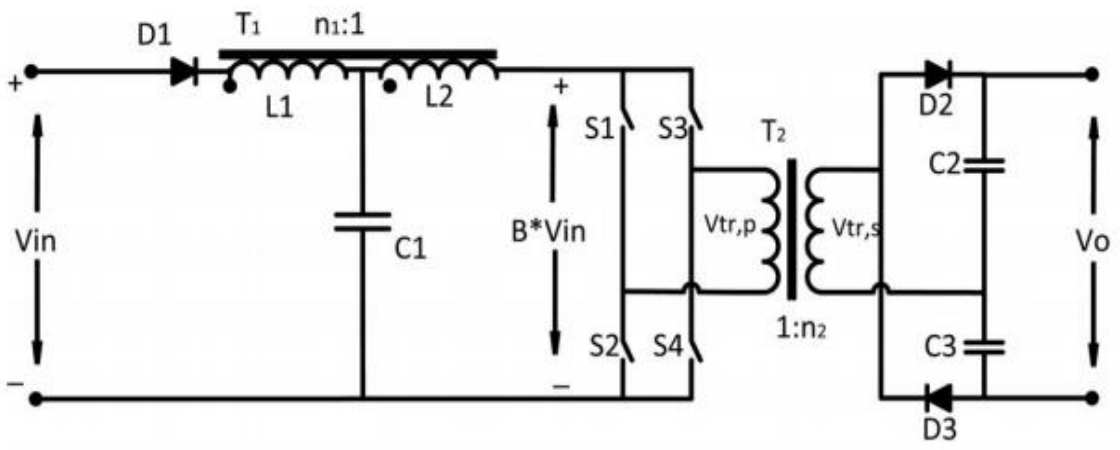


Figure 2.8 trans-Z-source DC–DC converter

An isolated Z-source DC-DC converter is presented in (Evran and Aydemir, 2013; Evran and Aydemir, 2014) using coupled inductors. According to this topology, with the small shoot-through time period, high voltage gain is achievable and one of the

advantage of this topology is the minimum possible device stress. A new DC-DC converter topology called a Z − H converter inspired from a ZSI is presented in (Fan et al., 2008) by eliminating the frontend diode as shown in Figure (2.9).

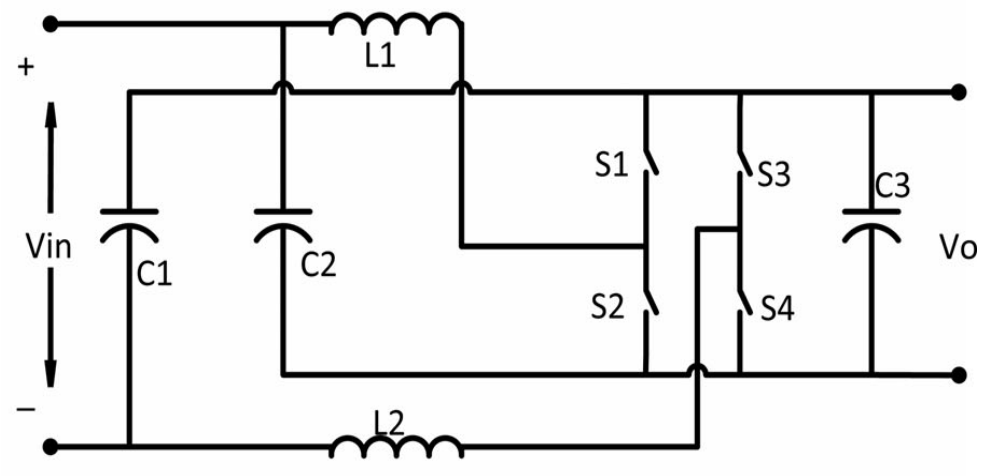


Figure 2.9 Trans-Z-source converter: Z − H DC–DC converter

In the simple duty cycle control of the switches, output voltage is controllable with the use of shoot-through time period. By changing the duty cycle in the range of 0-0.5 and 0.5-1 the converter could achieve two and four quadrant respectively; but, the boost factor is going to be the same in all traditional z-source inverter's operation modes.

A family of four-quadrant DC-DC converters using a Z-source/quasi-Z-source network with a minimum number of switches and passive devices is presented in (Dong and Peng, 2009). These converters employ a Z-source/quasi-Z-source network with two active switches to provide four quadrant operation; which means, bipolar output voltage and bidirectional current operation. Figure (2.10) shows a Family of four-quadrant DC-DC converters using Z-source and quasi-Z-source network.

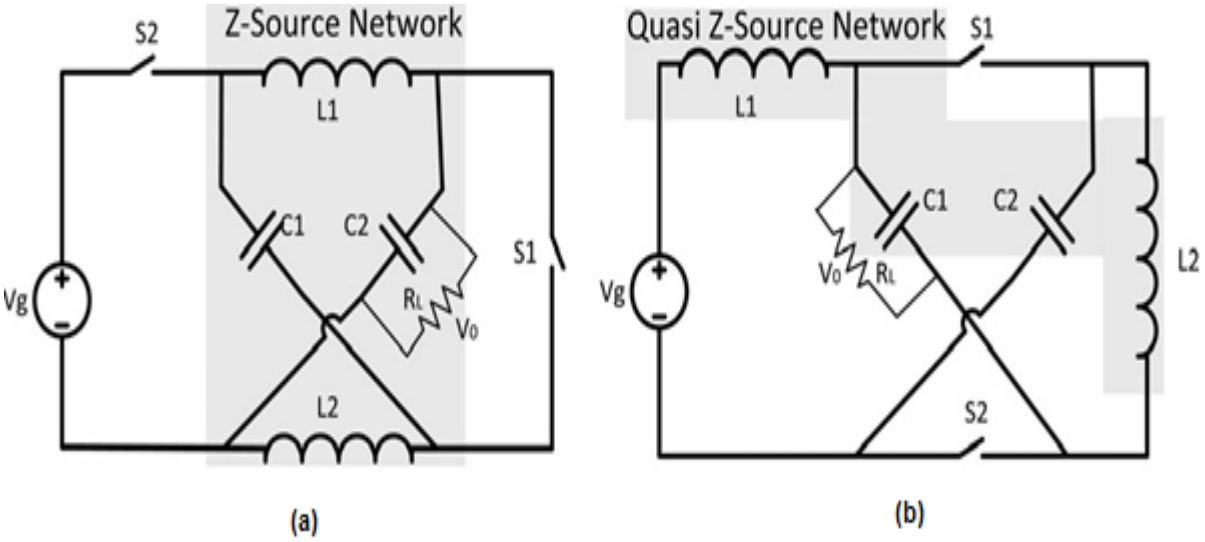


Figure 2.10 Family of four-quadrant DC–DC converters using (a) Z-source and (b) quasi-Z-source network

The converter has both buck/boost characteristics in the 0–1 range of the duty cycle. This feature along with changing the polarity of the load voltage by just controlling the duty cycle of the switch makes the converter very simple and more economical for many applications, e.g., DC-drives and other renewable energy systems. A new boost DC-DC converter topology is proposed in (Siwakoti et al., 2014a) with three coupled inductors called a Y-source converter. With the help of this converter topology and minimum shoot-through time period, higher boost voltage is achievable. The design of this converter is very well-set with lower rating to achieve higher voltage boost. Y-source impedance network based isolated boost DC-DC converter is presented in (Siwakoti et al., 2014b) with reducing the complexity of the switches and switching devices.

As well as the previous DC-DC converter topologies different type of DC-DC converters are widespread in the literature, e.g., a bidirectional Z-source DC-DC

converter (Xupeng and Xingquan, 2008), an isolated bidirectional with a bivariate coordinated control strategy (Biao et al., 2012), a resonant (Honnyong et al., 2010) and Z-source DC-DC converter with common ground (Asano et al., 2011). The voltage stress and power rating of the devices can be reduced with cascade (Vinnikov et al., 2012)and series-in parallel-out (Martinez et al., 2012) topologies. However, this increases the size, cost and complexity of the control system.

2.2.2 DC–AC Inverter Topologies

Two-level H-bridge, multilevel/neutral-point clamped (NPC), and the dual bridge are the converter topologies which originated from basic converter topologies using the fundamental properties of the impedance source network. As shown in Figure (2.6) the retrofitting of these various traditional topologies produces a new converter with an improved performance and reliability. Moreover, all control techniques and pulse width modulation by modifying the shoot-through time period are still valid. Various converter topology and different modification deliberated in the following sections.

2.2.2.1 Two-Level H-Bridge Topologies

The impedance source network was originally implemented with a three-phase H-bridge switching topology as voltage source and current source to demonstrate its superiority over the conventional VSI and CSI. Both single-phase as well as three-phase inverters can be implemented with an impedance source using the H-bridge circuit. There are numerous topologies and architectures for PV, fuel cell, super-capacitor, battery bank, grid-connected drives as well as uninterruptible power

supply UPS systems (Liming et al., 2011); Figure (2.11) shows a general impedance-source inverter for one-phase or three-phase.

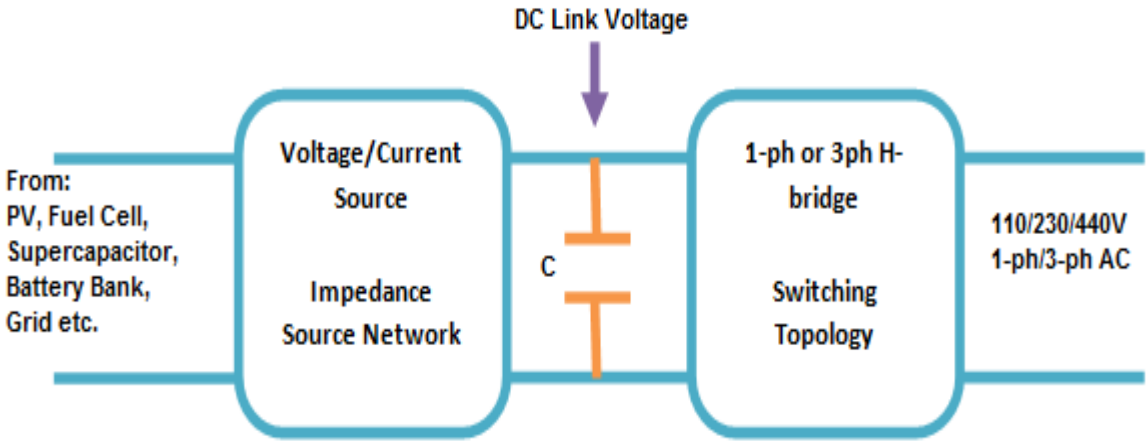


Figure 2.11 General impedance-source inverter for one-phase or three-phase

A new inverter topology is proposed in (Yu et al., 2011b);which input and output has a common ground. This single phase z-source inverter only operates with two switches and one-cycle control technique. It has the voltage transfer ratio as the full-bridge inverter. This topology is appropriate for distributed power system where dual grounding between source and load is required.

A two-level switched boost inverter similar to the Z-source inverter is proposed in (Ravindranath et al., 2013). The topology of switched boost inverter (SBI) by modifying a shoot-through time period across the inverter bridge will boost the output voltage. Reducing the number of passive components and increasing the number of active components are the advantages of this topology in comparison with Z -source inverter.

2.2.2.2 Multilevel/NPC

The concept of utilizing multiple small voltage levels or a split capacitor bank to perform power conversion by using a multilevel approach is prevalent in the literature. The advantages of this multilevel approach compared to two levels include premium power quality, excellent electromagnetic compatibility (EMC), low switching losses, and high voltage capability. However, larger numbers of switching semiconductors are required to implement it, along with a complex control system. In addition, small voltage steps must be supplied on the DC side, either by a capacitor bank or by isolated voltage sources. The concept of this multilevel approach is being adopted with an impedance source network to overcome some of the disadvantages of the classical multilevel topologies.

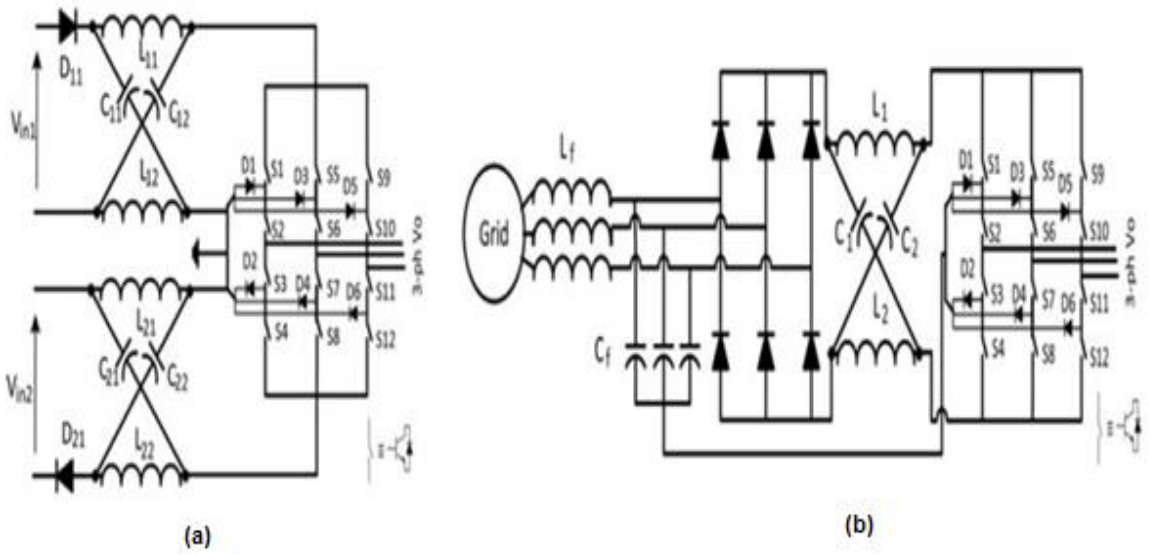


Figure 2.12 various impedance-network-source multilevel converter topologies: (a) two source NPC, (b) single-source NPC

To reduce the commutation and harmonic distortion of the system, different topologies with unique modulation techniques for controlling the multilevel converter is implemented. Figure. (2.12(a)) shows a three-level NPC converter using two ZSIs (Poh Chiang et al., 2007b). The neutral point is connected to a common point of the two ZSIs and is grounded. There are other topologies implemented with reduced number of passive (Poh Chiang et al., 2009) and active devices (Banaei et al., 2012) to reduce the size and cost of the system as can be seen in Figure. (2.12(b)). A QZSI based NPC topology is also presented in (Husev et al., 2012) with a modified modulation technique as can be in seen Figure (2.13(a)). Recently, a seven-level single-phase grid-tied inverter was proposed for a PV system using a cascaded multilevel QZSI topology (Yushan et al., 2014b) as shown in Figure (2.13(b)).

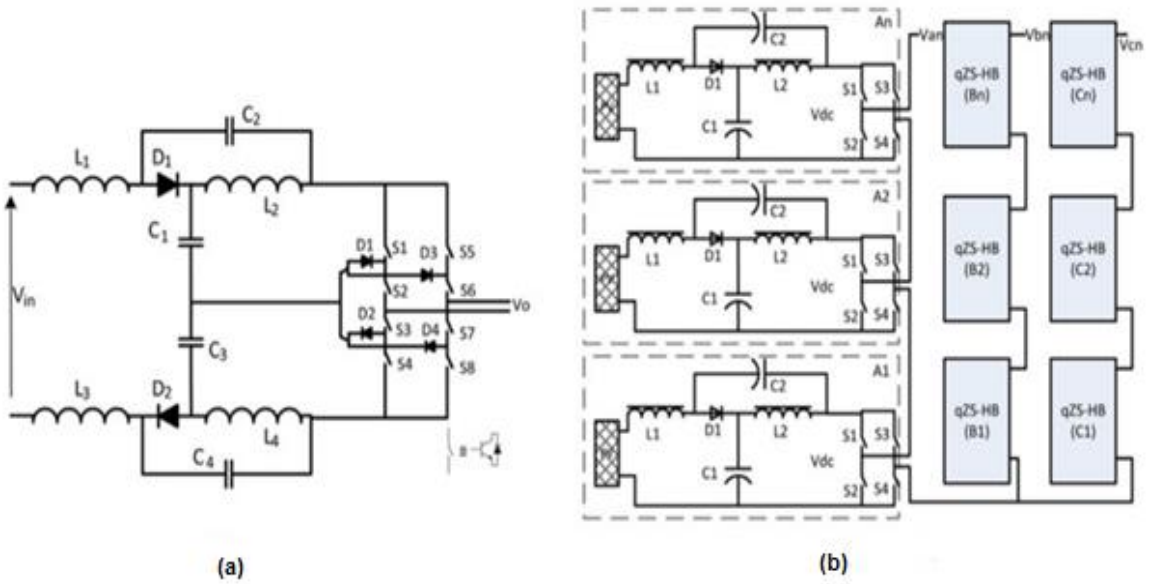


Figure 2.13 (a) single-source quasi-Z-source and (b) cascaded multilevel QZSI topology

This topology with the unique control technique and voltage control loop accomplishes maximum power point tracking per photovoltaic panel distinctly; also the voltages of the DC-link in each H-bridge module will be balanced.

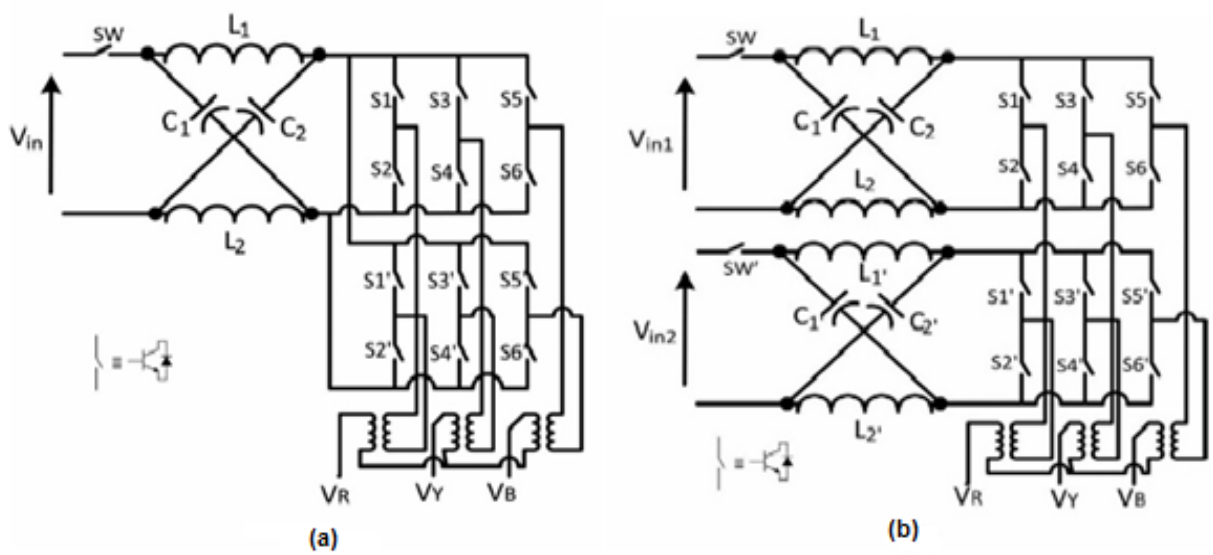


Figure 2.14 Dual ZSI with three-level reduced common mode switching: (a) with single source and (b) with two isolated sources

A three-level impedance-source inverter can also be implemented using a traditional dual H-bridge concept. A three-level inverter for motor drives is realized using two cascaded ZS VSIs and a three-phase transformer in (Feng et al., 2007). The inverter can supply to generic Δ or Y-connected loads with a single or two isolated DC sources as shown in Figure. (2.14).

2.2.3 AC–AC Converter Topologies (Matrix Converter)

AC-AC converter (matrix) is a direct converter topology consists of nine bidirectional switching devices which authorise any output and input phase to be linked and power factor can be controlled.

Figure. (2.15) shows impedance-source network-based matrix converter. The advantages of new matrix converter topology can overcome the limitation of basic matrix converter (Baoming et al., 2012; Kiwoo et al., 2012), which the voltage gain could not be greater than 0.866 because of switches being vulnerable in the shoot-through time period.

A combination of impedance network with basic matrix converter can be operated as a buck or boost with a vast range of output voltage and frequency for AC load which requires variable voltage and frequency.

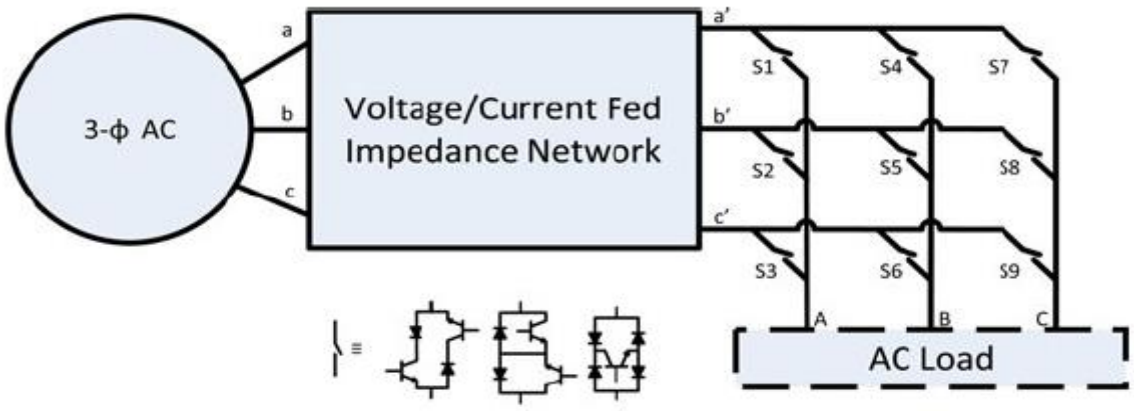


Figure 2.15 Impedance-source network-based matrix converter: general topology

To enhance the reliability and efficiency of the converter various control techniques and pulse with modulation methods, e.g., simple maximum boost control, maximum boost control, maximum gain control, and hybrid minimum stress control have been presented in (Xiong et al., 2012; Qin et al., 2012).Single-phase Z-source AC-AC converters (Minh-Khai et al., 2010; Dehghan et al., 2010) and single-phase

quasi-Z-source AC-AC converters sharing a common ground (Minh-Khai et al., 2012; Minh-Khai et al., 2009) with the load are also presented with suitable PWM techniques.

2.2.4 AC-DC converter topologies

AC-DC (Rectifiers) topologies have the ability of operating in a buck-boost mode in a single stage, also providing less distortion in each line current, good input power factor, enhanced efficiency and reliability. A Z-source inverter (Xinping et al., 2006), and quasi-Z-source (Konga and Gitau, 2012) based on rectifier topologies are presented as shown in Figure (2.16).

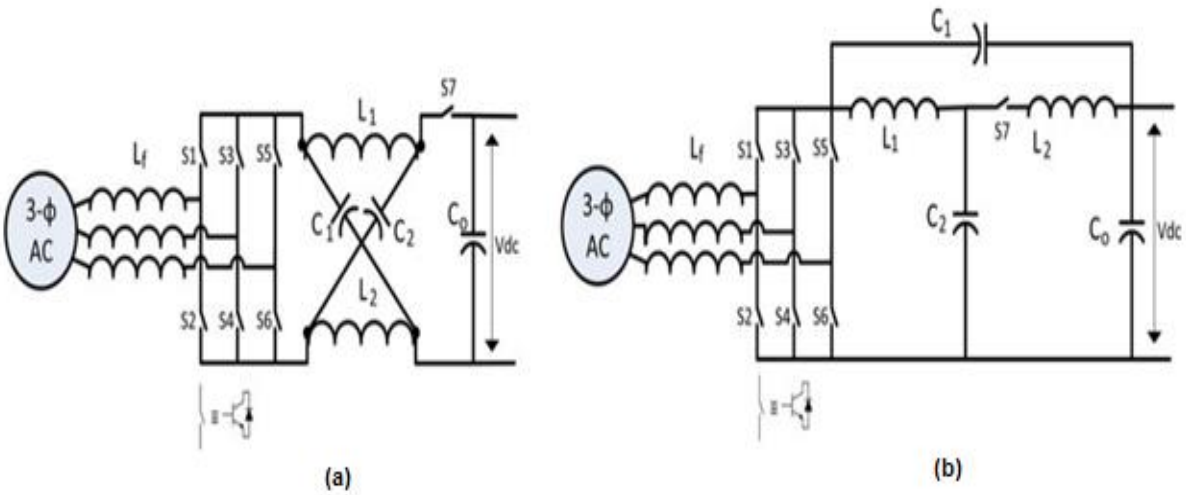


Figure 2.16 AC–DC rectifier topologies based on (a) ZSI and (b) QZSI impedance network

A new concept of a bidirectional converter based on a matrix converter is also presented in (Keping and Rahman, 2009). The advantages of the AC-DC matrix converter are controllable input power factor, tight DC voltage regulation, wide

bandwidth with quick response to load variations, and single-stage buck voltage AC-DC power conversion.

2.3 Electric Power Conversion Topologies

All electric power conversion topologies inspired from impedance-source network with reorganizing LC components (Anderson and Peng, 2008; Shuai and Peng, 2011). Figure (2.17) shows the impedance-source network topologies which categorized as a non-transformer and transformer based.

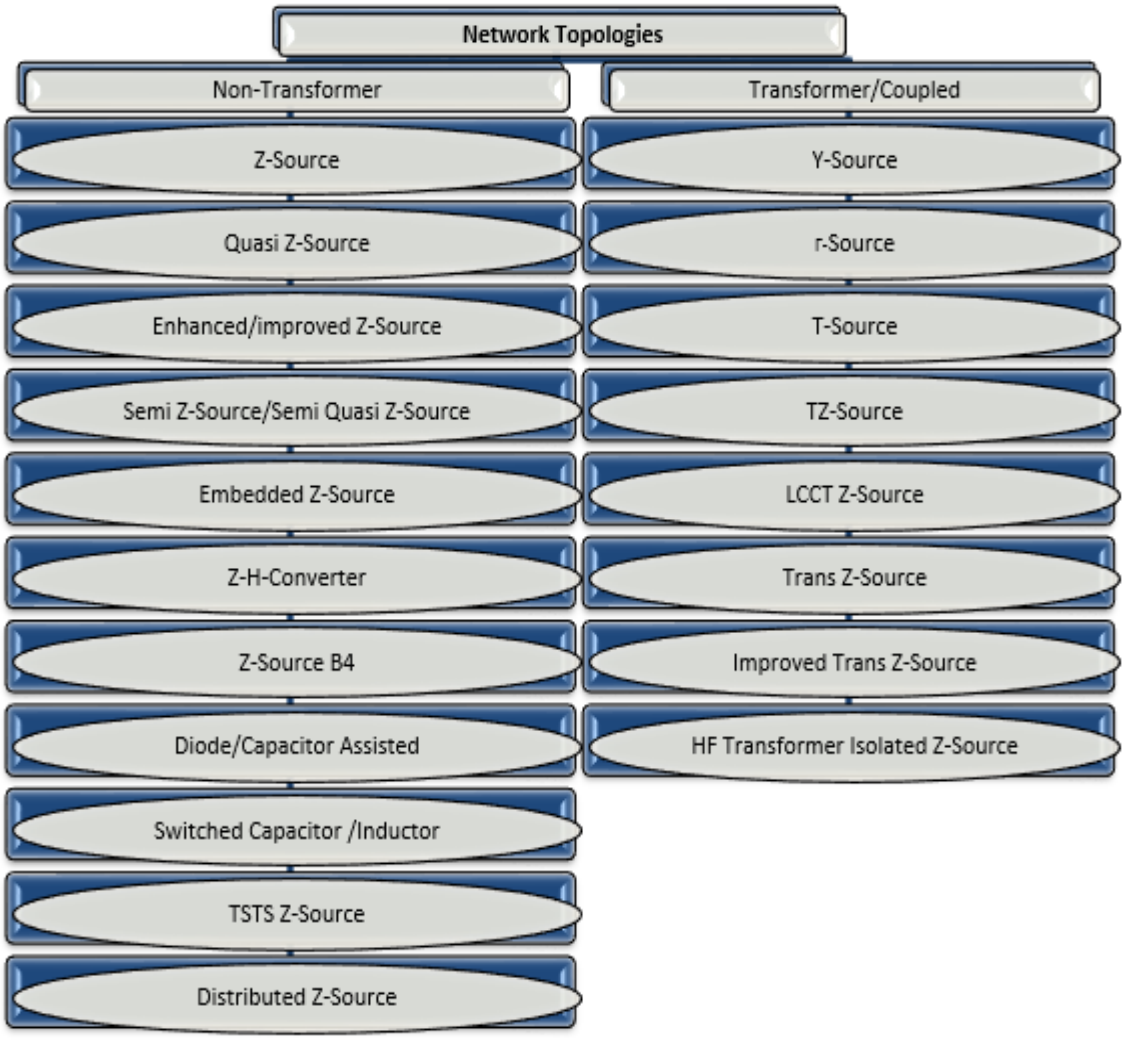


Figure 2.17 Impedance-source network topologies

Modifying the impedance source circuit can produce distinct trait for various application's need; moreover, by mixing the basic switched inductor/capacitor, tapped inductor and with the help of diode and capacitor addition to the network can increase the network's voltage. Unique properties of each topology will be discussed in the following sections.

2.3.1 Non-transformer based

2.3.1.1 Z-source / QZ- source

Generally Z-source/QZ-source inverters categorised into voltage fed and current fed; however, unlike the traditional voltage-fed/current-fed inverter, the impedance-source network provides a buffer between the source and the inverter bridge; and facilitates a short and an open-circuit at any time depending on the mode of operation.

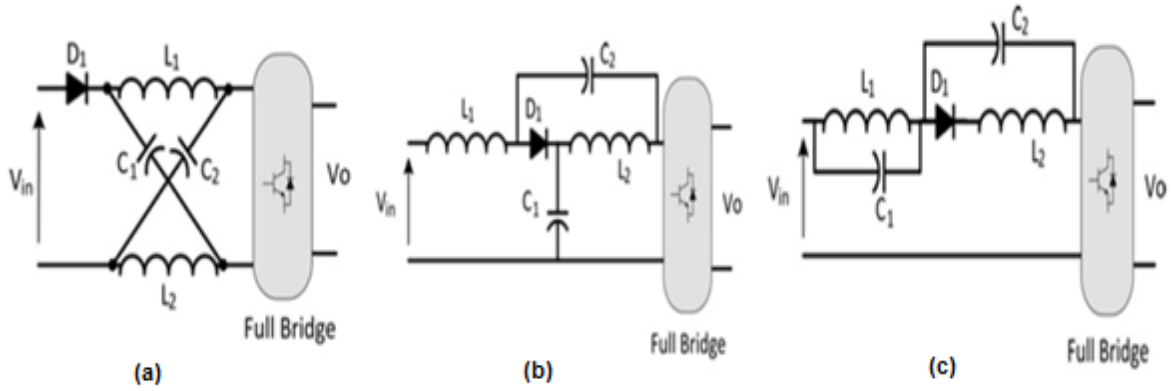


Figure 2.18: various voltage-fed ZSI topologies: (a) ZSI with discontinuous input current, (b) QZSI with continuous input current, and (c) QZSI with discontinuous input current

Traditional voltage-fed/current-fed Z-source impedance networks suffer from problems like discontinuous input current in the boost mode of the voltage-fed-ZSI [See Figure (2.18(a))] and high current stress on the inductor in the current-fed-ZSI [See Figure (2.19 (a))].

As can be seen in Figure(2.18(b)) and (c) and Figure(2.19(b)) and (c) different topologies has inspired from Z-source and quasi-Z-source inverters as a voltage fed and current fed source with improved efficiency and reliability, which presented in (Shuitao et al., 2011; Poh Chiang et al., 2008) to solve the problem of z-source inverter (Yu et al., 2014).

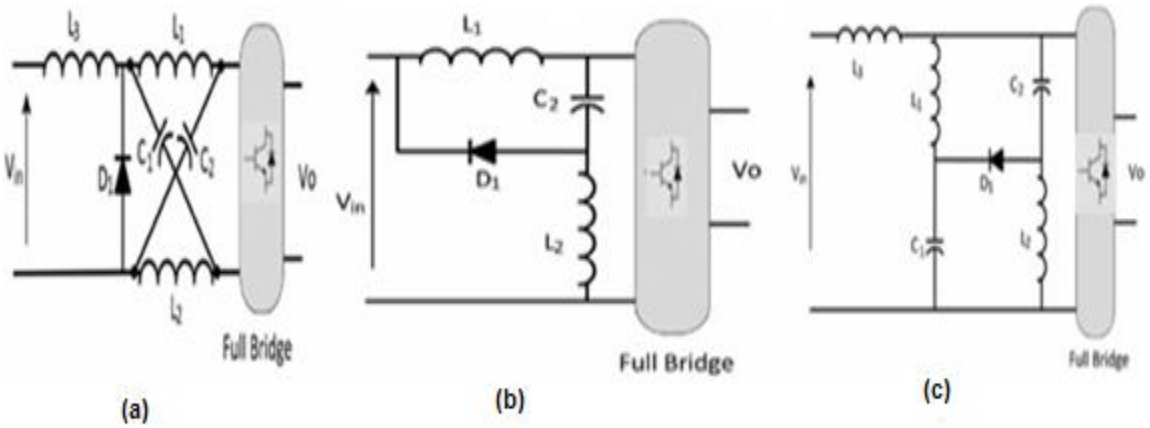


Figure 2.19: various current-fed ZSI topologies (switches have to be reverse-blocking devices): (a) ZSI with continuous input current, (b) QZSI with discontinuous input current, and (c) QZSI with continuous input current

As shown in Figure (2.19(a) –(c)) all current-fed-z-source-inverters can be operated in buck–boost mode and has the capability of being bidirectional for power flow. However the reverse blocking of the switches is compulsory. These new advantages will expand this converter topology for various renewable energy applications, i.e.

Wind, PV, and motor derives, (Peng, 2002; Yu et al., 2011b; Joel Anderson, 2008; Yushan et al., 2013).

2.3.1.2 Enhanced/ improved z-source

There are different topologies and modulation techniques to enhance the boost capability contained by Z-source and QZ-source networks. In the same framework, an enhanced-boost ZSI is proposed in (Ding et al., 2013; Weihai, 2013) with alternate-cascaded switched and tapped-inductor cells using some lower rated components. Similarly, an improved Z-source (Yu et al., 2011a; Yu et al., 2009b) and an improved trans-Z-source (Minh-Khai et al., 2013a) are proposed, respectively, to reduce the capacitor voltage stress. Basic Z-source and quasi -Z-source inverters have some problems which can be solved and overcome with these topologies; on the other hand, the cost of the converter system will increase as well as decreasing the power density.

2.3.1.3 Semi-Z- source /semi quasi-Z-source

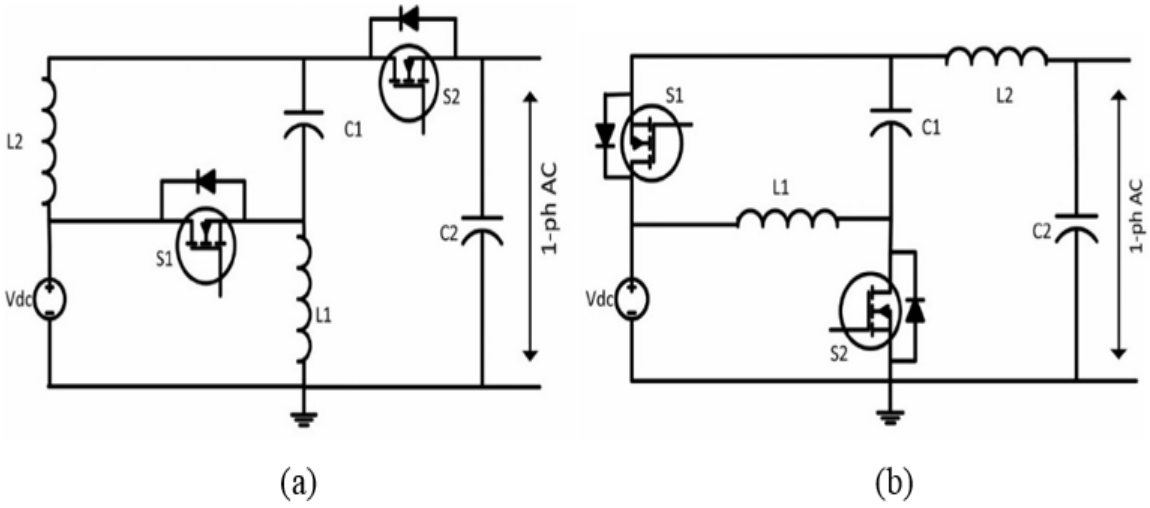


Figure 2.20 Semi-Z-source topologies: (a) Semi-ZSI and (b) semi-QZSI(Dong et al., 2011b)

To achieve low cost and high efficiency in applications such as single-phase grid-tie PV power systems, new topology called semi-Z-source inverters is proposed as shown in Figure (2.20).

Non-isolated semi-Z-source inverter have an advantages of using fewer switches and no shoot-through zero state in comparison to the basic Z-source and quasi-Z-source, also by use of two active switches of the ZSI/QZSI provides a voltage boost as well as sharing the same ground between input DC and output AC voltage, which leads to low leakage current (Dong et al., 2011b; Dong et al., 2011a). In addition, the cost of the system will be less to compare with traditional ZSI/QZSI. The disadvantage of this inverter is the high capacitor voltage stress in comparison to the basic ZSI and QZSI (Haimovich et al., 2013). For the application such as photovoltaic using of this topology is preferable.

2.3.1.4 Embedded z source

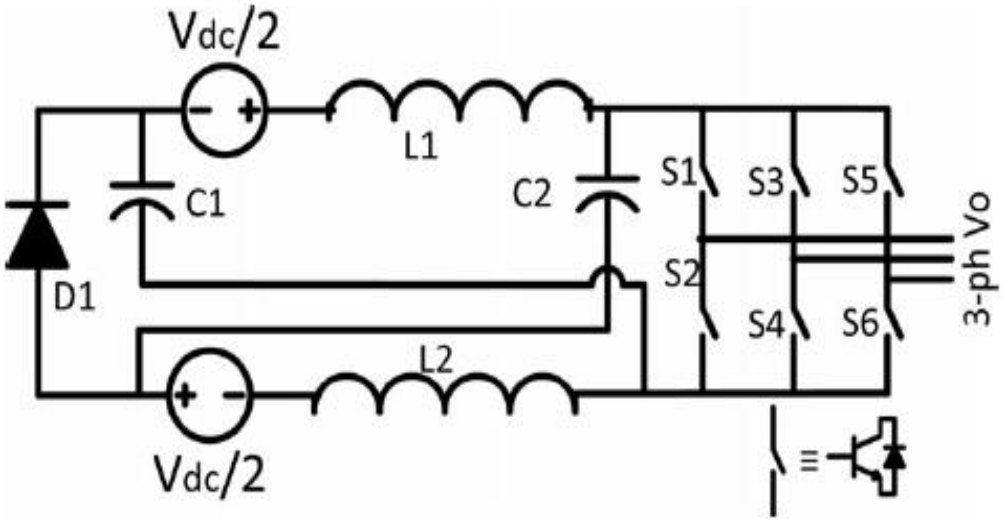


Figure 2.21 Two-level-embedded ZSI

The embedded-Z-source topology without employing any extra passive filter as an advantage, can provide the same gain as traditional Z-source inverter. The unique properties of this topology is appropriate for photovoltaic system (Poh Chiang et al., 2010; Gao et al., 2008).

A two level embedded Z-source topology is shown in Figure (2.21). Some other embedded Z-source topologies can be usable for battery storage systems with one/two DC sources.

2.3.1.5 Z-H converter

The Z-H converter has inspired from traditional ZSI by eliminating the input diode and no shoot-through time period of switches (Fan et al., 2008). The gain of the converter is similar to that of the Z-source network but it has two modes of operation, i.e., boost mode in duty cycle D = [0- 0.5] with positive output voltage and boost mode in D = [0.5- 1] with negative output voltage. Usually, the Z-source inverter works within D= [0-0.5], and the magnitude of the output voltage can be infinite when D is close to 0.5. Therefore combined with the modulation index of the inverter part, the Z-source inverter can provide any desired voltage theoretically. This converter topology can be applied for different power conversion systems i.e. (DC-DC), (DC-AC), (AC-DC) or (AC-AC).

2.3.1.6 Z-Source B4 Converter

A new Z-source B4 inverter topology has inspired from basic B4-Voltage-source inverter.(Poh Chiang et al., 2007c) This inverter with less active elements can be

operated with no dead-time protections, which lead to enhance the reliability and reduction of cost. Figure (2.22) shows the Z-source B4 converter topology for a three-phase power conversion.

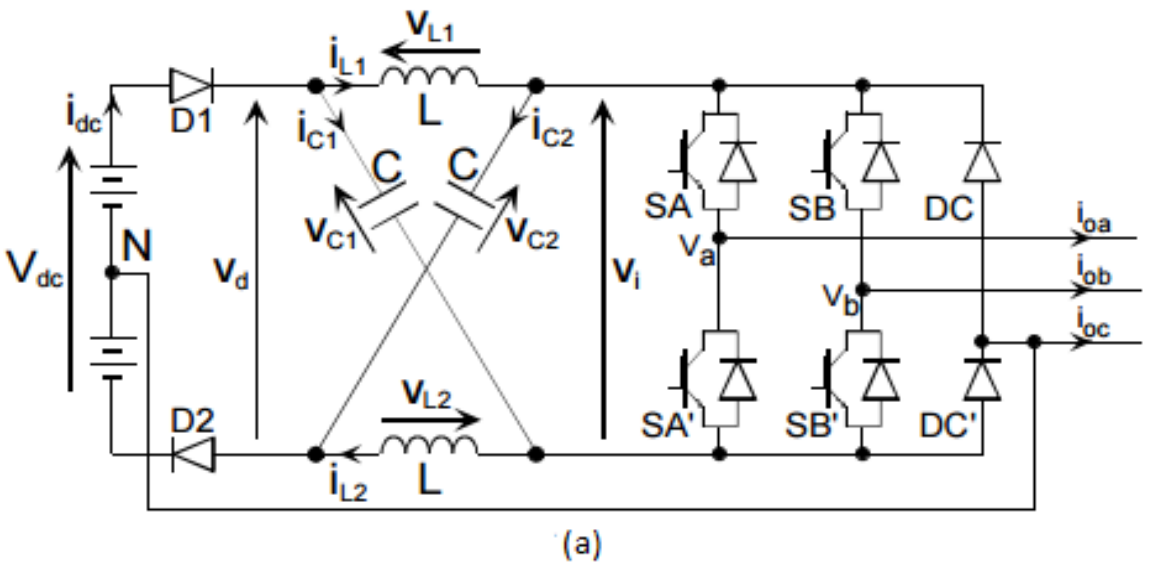


Figure 2.22 B4 ZSI topology

2.3.1.7 Switched Inductor/Capacitor

Extra inductors and capacitors have been added in the Z-source and quasi-Z-source impedance network, aim of improving the boost capability of the circuit. Many topologies are presented in the literature to reduce the stress on the passive components and also to eliminate the start-up inrush current. A switched inductor/capacitor ZSI/QZSI provides continuous input current and reduced voltage stress on the capacitor (Miao et al., 2010; Nguyen et al., 2012). Small shoot-through time period is needed to generate large output voltage.

An embedded-Z-source with a switched inductor combines the advantages of both topologies, e.g., high boost ratio, reduced capacitor voltage stress, and low input ripple

current (Itozakura and Koizumi, 2011). However, this switched inductor/capacitor topology needs large number of passive devices, which increases the cost and volume of the converter.

2.3.1.8 Capacitor/Diode Assisted

According to different applications requirements, voltage boost can be increased by adding additional capacitor and diodes to the conventional QZ/Z-source inverters to achieve the highest voltage boost (Gajanayake et al., 2010; Gajanayake et al., 2009). As shown in Figure (2.23) the quasi-Z-source extended by adding a diodes and capacitors.

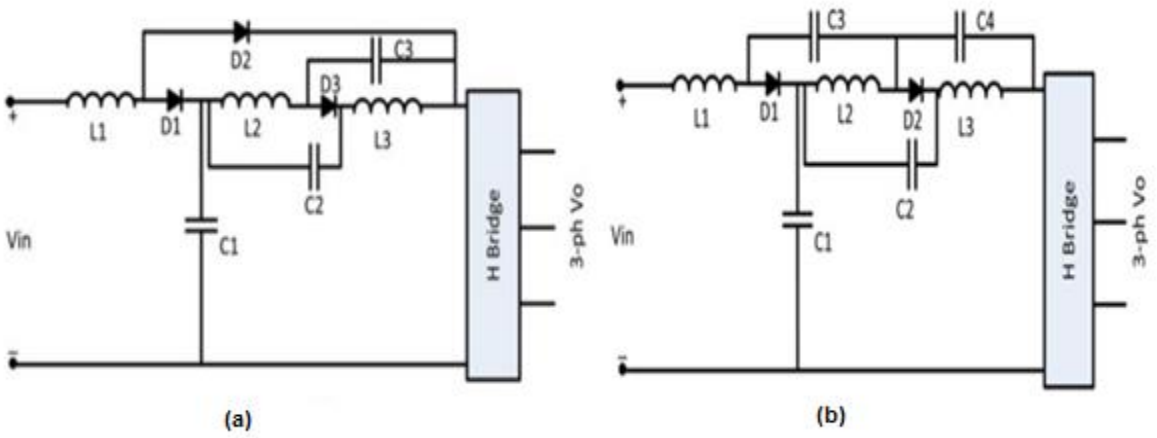


Figure 2.23 Assisted QZSI topologies: (a) diode assisted and (b) capacitor assisted

These topologies have high voltage gain as well as lower capacitor stress; though, the cost will increase because of added passive elements.

2.3.1.9 Three-Switch Three-State (TSTS) Z-Source

Three switch three-state single-phase ZSIs (TSTS-ZSIs) were proposed recently in (Long et al., 2013), and it can be categorized into boost and buck based TSTS-ZS Inverters as shown in Figure (2.24). As an advantages, in comparison to the conventional topologies, utilizing less switches can increases the power density and decreases the switching stress as well as sharing the ground which make an appropriate topology for any photovoltaic PV systems.

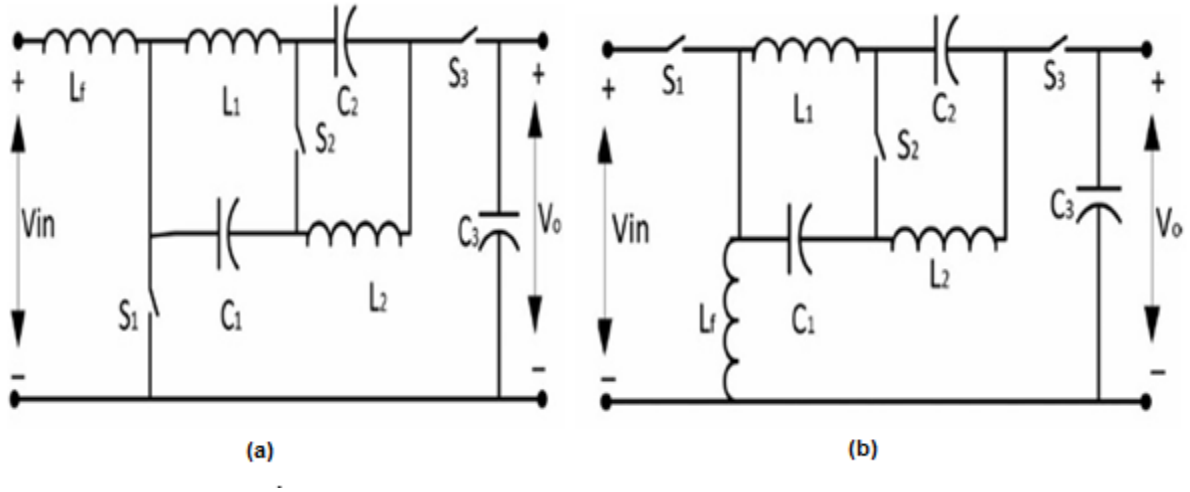


Figure 2.24 TSTS-ZSIs: (a) boost topology and (b) buck–boost topology

2.3.1.10 Distributed Z-source

Distributed impedance networks such as transmission lines and hybrid LC components can be used for a Z-source network (Peng, 2008; Shuai and Peng, 2011) as shown in Figure (2.25). These distributed Z-source networks are difficult to implement, but a distributed ZSI does not need any extra diode or switch to achieve the voltage boost function, therefore, minimum component count. This topology could open a door for an impedance-source network to radio-frequency power converter

design by utilizing the distributed inductance and capacitance prominent at higher frequencies.

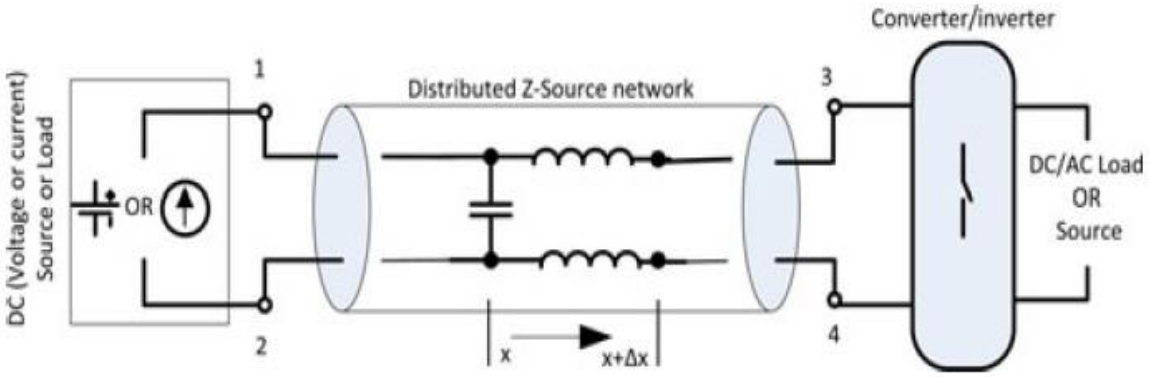


Figure 2.25 General topology of a distributed Z-source converter

2.3.2 with Transformer or Magnetic Coupling

To reduce the concern of voltage stress on the switches in the high DC-link voltage, a new topology “magnetic coupling” is introduced (Poh Chiang and Blaabjerg, 2013). The new topology has improved the voltage boost along with modulation index. In order to have a better power density, a generic methodology utilizes less passive elements to reduce the cost of the system. The following sections describe the impedance network topologies based on transformer or coupled inductor.

2.3.2.1 Y-source

The Y-shaped impedance source network (Siwakoti et al., 2014b) presenting an inimitable impedance network utilizing small duty ratio to have large output voltage boost. The network includes coupled transformer along with 3 windings. The generated gain has not matched with existent network at the same operation time and

duty ratio. Any output voltage boost is achievable by regulating shoot-through time period and turns ratio.

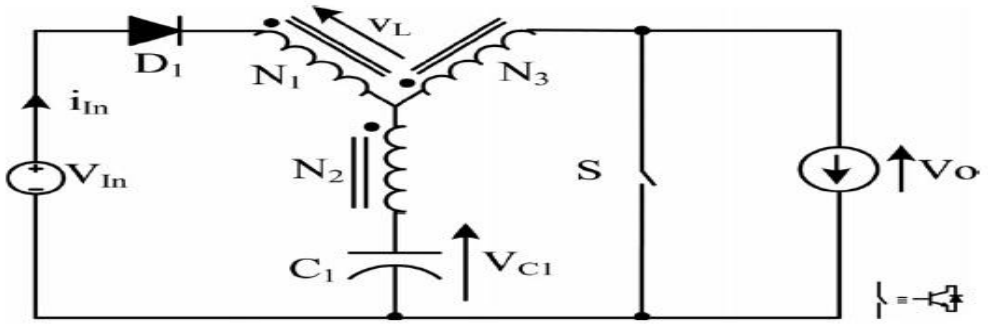


Figure 2.26 Basic Y-source impedance network for power conversion

The Y-shaped impedance source network for electric power converter can be seen in Figure (2.26).

2.3.2.2 Γ-shaped Z-source inverter

The Γ-shaped Z-source inverter utilizing coupled inductors with great voltage boosting and modulation ratio proposed in (Poh Chiang et al., 2013; Poh Chiang et al., 2012b), which make the device cost effective by using less component.

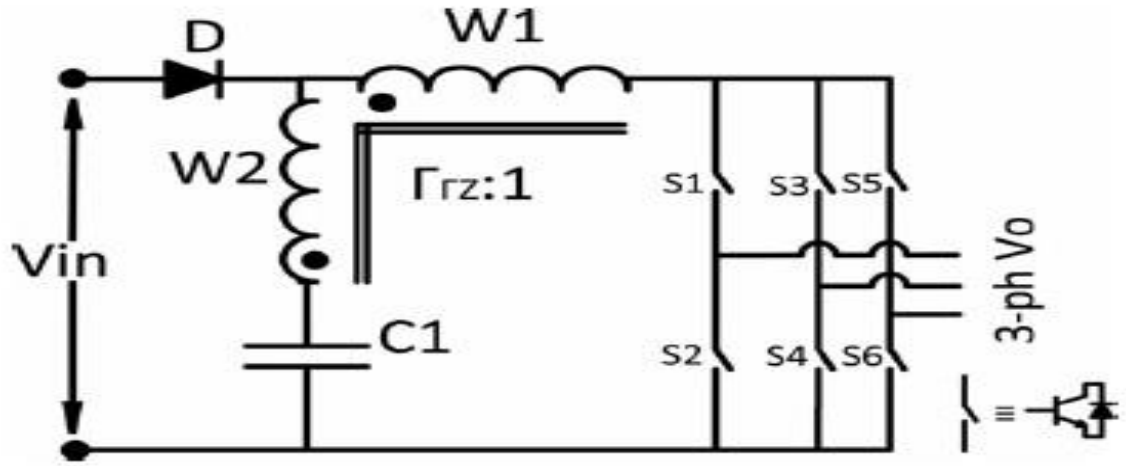


Figure 2.27 Γ-Z-source network topology

In comparison with other transformer-based networks with having a high gain and turns ratio, the Γ shaped Z-Source, increases the gain and reduce the turn's ratio. Figure (2.27) shows the Γ-Z-source network topology for an inverter.

2.3.2.3 T-source

The T-shaped inverter using a capacitor along with coupled inductor (Strzelecki et al., 2009; Sheeja P.Kumar, 2012) shows in Figure (2.28). The network with few reactive components has substantial advantages in utilizing common voltage source of the passive arrangement, which makes a suitable topology for neutral point clamped converters. The gain of the T-shaped source inverter can be set high, compared with conventional QZ/Z-source inverters.

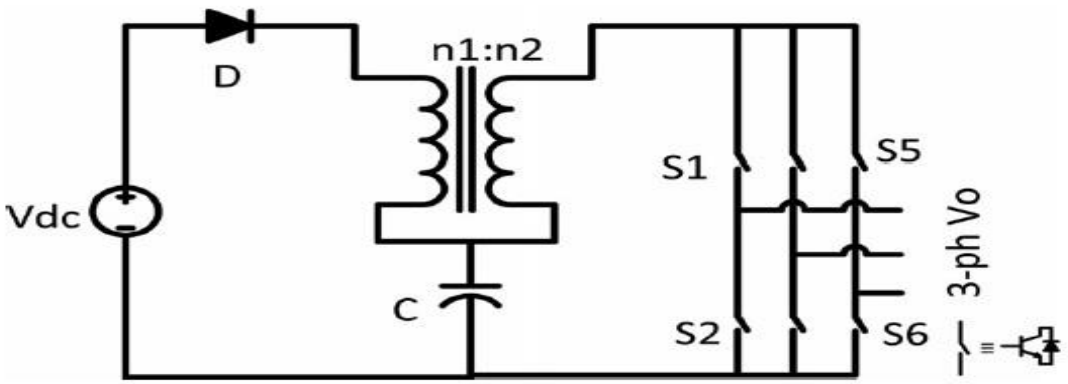


Figure 2.28: T-source network topology

2.3.2.4 Trans Z-source inverter

The Trans Z-source inverter including coupled inductors and one capacitor (Wei et al., 2011) and parallel operation of Trans-Z source (Dongsul et al., 2011)

producing high voltage gain and less voltage stress in the switches compared with conventional QZ/Z-source inverters. In theory, the original Z-source, QZ-source, and embedded Z-source have illimitable voltage gain. But actually having a great voltage gain causes high voltage stress. Figure (2.29) shows the Trans-Z-source inverter.

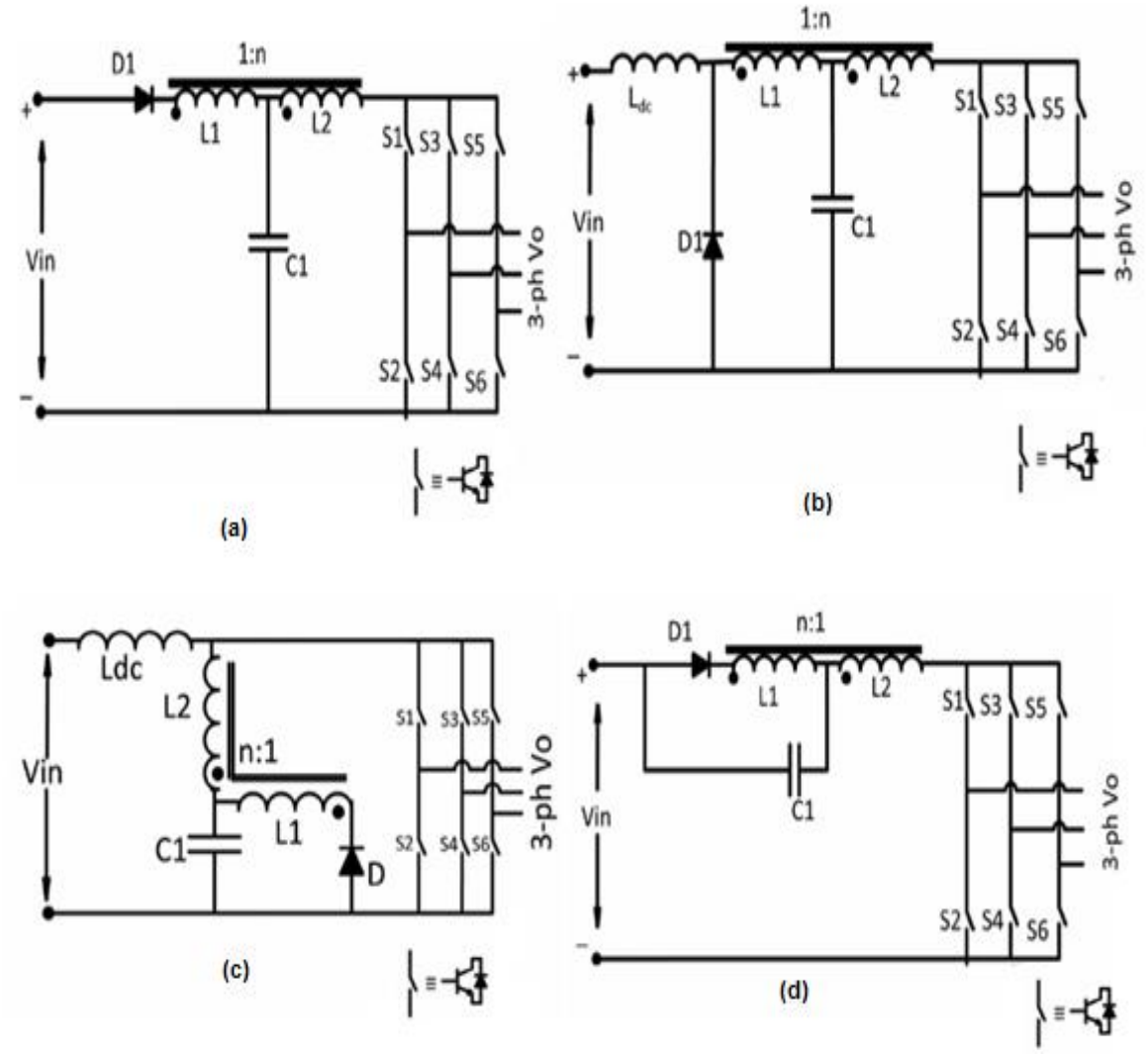


Figure 2.29 Trans-ZSI: (a) voltage-fed trans-Z-source, (b) current-fed trans-Z-source, (c) current-fed trans-quasi-Z-source, and (d) voltage-fed trans-quasi-Z-source

2.3.2.5 TZ-source inverter

In order to increase the voltage gain, TZ-source inverter presented in (Minh-Khai et al., 2013b) with the turns ratio more than 1 which in comparison with Trans-Z-source inverter has lesser transformer turns ratio. The TZ-source includes of two transformer instead of two inductors along with the rest of passive component as same as conventional Z-source inverters which increases the cost of the system. Figure (2.30) shows the circuit topology of the TZ-source network for a three-phase inverter.

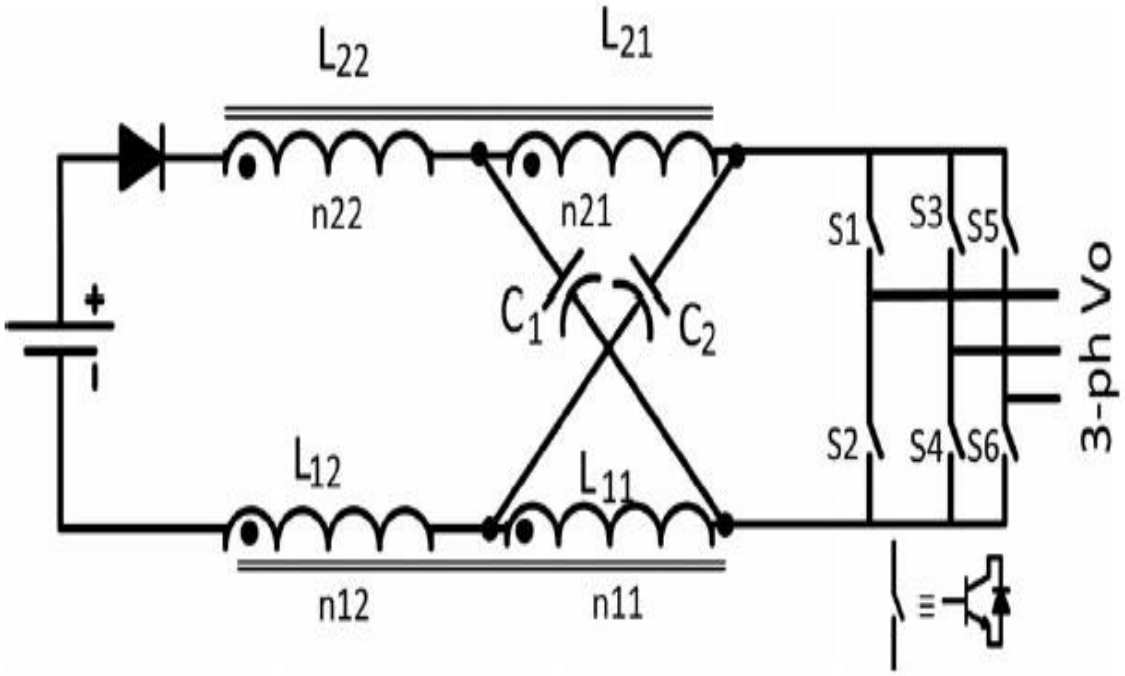


Figure 2.30 TZ-source network topology

2.3.2.6 LCCT Z-Source

The LCCT Z-source with the inductor and a transformer integrated into a common core, as shown in Figure (2.31), achieves higher voltage gain and modulation index (Adamowicz et al., 2011b; Adamowicz et al., 2011b). This topology maintains a

continuous input current even at a light load, and also filters out high-frequency ripples from the input current.

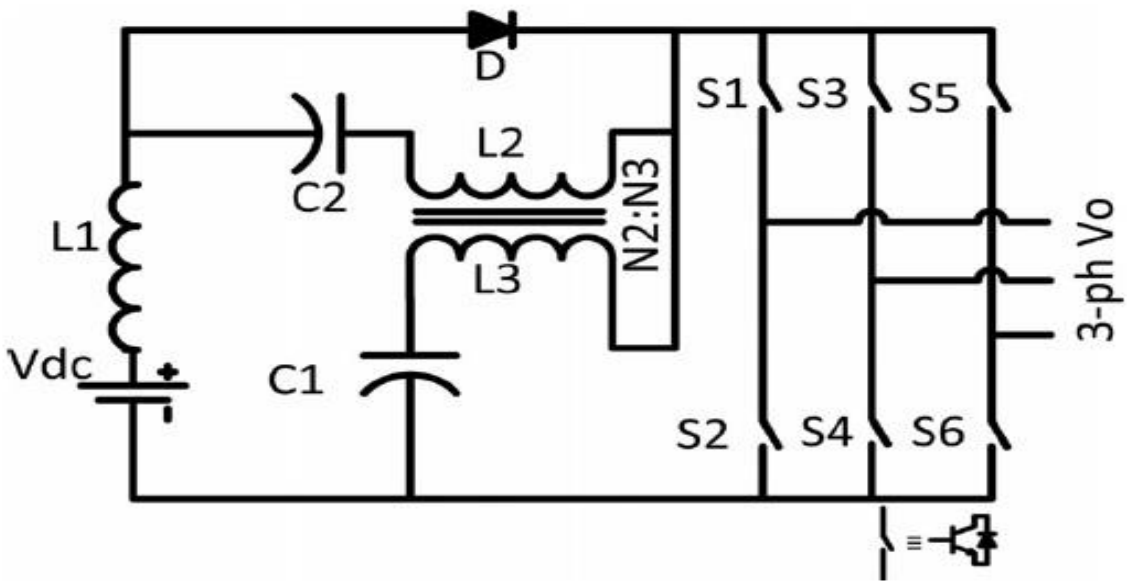


Figure 2.31 LCCT network topology

2.3.2.7 HF Transformer-Isolated Z-Source/Quasi-Z-Source/ Trans-Z-Source

A family of impedance-source networks with intermediate HF isolation is presented with different topologies for applications requiring isolation for safety reasons (Shuai et al., 2011). These topologies inherit all the benefits of the Z-source networks along with a higher boost ratio and lower device stress. However, this topology increases the number of active and passive components. In addition, the coupled transformer must be designed properly to minimize the leakage inductance. One example of a voltage-fed HF-isolated ZSI is shown in Figure (2.32).

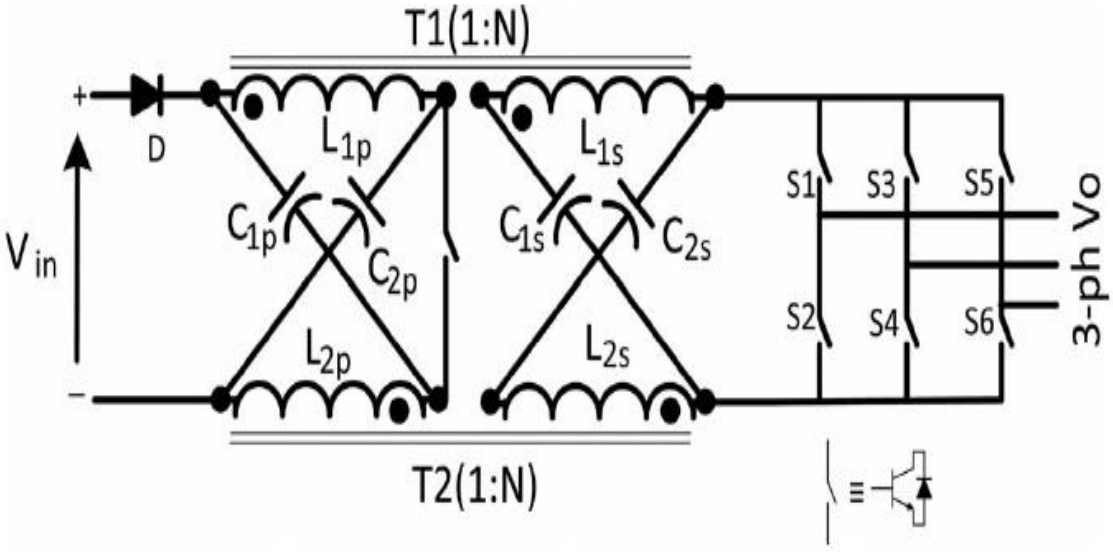


Figure 2.32 HF transformer-isolated ZSI

As discussed in the literature, there are different topologies proposed to overcome the disadvantages of conventional Z-source inverter. Table (2.1) summarizes the different impedance-source network topologies predominant in the literature.

Table 2.1 summary of impedance-source network topologies

Impedance Network Topology	Boost Factor	Voltage stress on the Switching Device	No.of Semiconductors	No.of Capacitors	No.of Inductors	Features
Z-Source(Peng, 2002)	$B=[1-2D_{st}]^{-1}$ Where,$0\leq D_{st}\leq 0.5, V_o>0$	$\frac{1}{1-2Dst}V_{in}$	1 Diode	2	2	Elementary circuit to overcome the conceptual and theoretical barrier of VSI and CSI that leads to many useful derived topologies. Discontinuous input current and higher voltage stress on capacitors. The inductor of current-fed ZSI must sustain high currents.

Quasi A-Source (Anderson and Peng, 2008)	$B=[1-2D_{st}]^{-1}$ Where,$0\leq D_{st}\leq 0.5, V_o>0$	$\frac{1}{1-2Dst}V_{in}$	1 Diode	2	2	First modification of Z-source network. Continuous input current. Reduced passive component ratings. Reduced component count.
Improved Z-Source (Yu et al., 2011a)	$B=[1-2D_{st}]^{-1}$ Where,$0\leq D_{st}\leq 0.5, V_o>0$	$\frac{1}{1-2Dst}V_{in}$	1 Diode	2	2	Reduced capacitor voltage stress. Limit inrush current at start up.
Semi Z-Source (Dong et al., 2011b),(Dong et al., 2011a) Semi Quasi Z-source (Haimovich et al., 2013)	B=[1-2d]/[1-d] Where, Vo>0, for 0≤d≤0.5, Buck and Vo<0, $\begin{cases}0.5<d\leq 2/3, Boost\\ 2/3<d\leq 1, Boost\end{cases}$	$\frac{1}{1-d}V_{in}$	2Switches	2	2	Reduced active components count. Lower cost. Higher voltage stress across switches compared to ZSI/qZSI. Eliminate leakage currents and suitable for grid-connected PV system.
Embedded Z-Source (Poh Chiang et al., 2010),(Gao et al., 2008)	$B=[1-2D_{st}]^{-1}$ Where,$0\leq D_{st}\leq 0.5, V_o>0$	$\frac{1}{1-2Dst}V_{in}$	1 Diode	2	2	Draws smooth current from the source without adding additional components or passive filter
Enhanced Z-Source(Ding et al., 2013)	SL Cell: $B=\frac{1+(\gamma SL-1)Dst}{1-(N\gamma SL+1)Dst}$ Where, $0\leq Dst\leq\frac{1}{N\gamma SL+1}$, Vo>0	$\frac{1+(\gamma SL-1)Dst}{1-(N\gamma SL+1)Dst}Vin$	N+3(γSL-1) (N+1) Where, N is no. of Cascaded n/w	2N	γSL(N+1)	Higher voltage conversion compared to ZSI/qZSI at small shoot-through duration. Increases the number of components (low power rated.)
	TL Cell: $B=\frac{1+\gamma TLDst}{1-[1+N(\gamma TL+1)]Dst}$ Where, $0\leq Dst\leq\frac{1}{1+N(\gamma TL+1)}$, Vo>0	$\frac{1+\gamma TLDst}{1-[1+N(\gamma TL+1)]Dst}Vin$	N+2(N+1) Where, N is no Of Cascaded n/w	2N	(N+1), Each with turns ratio γTL	

Z-H Converter(Fan et al., 2008)	$B=[1-2D]^{-1}$ Where,$0\leq D\leq 0.5$ for Vo>0 And $0.5\leq D\leq 1$ for Vo<0	$\frac{1}{1-2D}V_{in}$	4 Switches	2	2	Front-end diode eliminated. No shoot-through state for voltage boosting.
Z-Source B4(Poh Chiang et al., 2007c)	$B=[1-2D_{st}]^{-1}$ Where,$0\leq D_{st}\leq 0.5$,$V_o>0$	$\frac{1}{1-2Dst}V_{in}$	1 Diode	2	2	Reduce the number of active semiconductors. Simplify the control and gating circuitries.
Y-Source(Siwakoti et al., 2014b)	$B(K,Dst)=[1-KDst]^{-1}$ Where, K≥2 and $0\leq Dst\leq\frac{1}{K}$,Vo>0	$\frac{K-1}{1-KDst}Vin$	1 Diode	2	One inductor and one 2-winding coupled inductor	Versatile. More degree of freedom to choose the gain of the converter. Very high gain can be achieved with small shoot-through duty cycle. Higher voltage boost and higher modulation index can be achieved simultaneously. Reduce THD of the inverter.
Γ-Source (Poh Chiang et al., 2013),(Poh Chiang et al., 2012a)	$B=[1-(1+[n-a]^{-1})Dst]^{-1}$ Where, $0\leq Dst\leq[1+[n-1]^{-1}]^{-1}$ and 1<n<2 (decreasing), Vo>0	$\frac{1}{(n-1)[1-\left(1+1+\frac{1}{n-1}\right)Dst}Vin$	1 diode	1	Integrated two winding	Higher gain can be achieved by lowering the turn's ratio of coupled inductor. Better spectral performance at the inverter output.
T-Source (Strzelecki et al., 2009, Sheeja P.Kumar, 2012) Trans Z-Source (Wei et al., 2011),(Dongsul et al., 2011)	$B=[1-(n+1)Dst]^{-1}$ Where,$0\leq Dst\leq[n+1]^{-1}$, Vo>0	$\frac{n}{1-(1+n)Dst}Vin$	1 diode	1	Integrated two winding	Increases voltage gain compared to ZSI and qZSI. Fewer reactive components compared to ZSI and qZSI. Common ground with the load. Reduced component stress.

TZ-Source (Minh-Khai et al., 2013b)	$B=[1-(n+1)Dst]^{-1}$ Where, $0\leq Dst\leq[n+1]^{-1}$, Vo>0	$\frac{1+N1+N2}{1-(2+N1+N2)Dst}$	1diode	2	Two Integrated 2-windings	Produce higher voltage boost with N.
LCCT Z-Source(Adamowicz et al., 2011b),(Adamowicz et al., 2011a)	$B=[1-(n+1)Dst]^{-1}$ Where,$0\leq Dst\leq[n+1]^{-1}$, Vo>0	$\frac{n}{1-(1+n)Dst}Vin$	1 diode	2	One inductor and one 2-winding coupled inductor	Continuous input current even during light load. Filters out high-frequency ripple from the input current.
HF Transformer Isolated(Shuai et al., 2011)	$B=n[1-2Dst]^{-1}$ Where,$0\leq Dst\leq 0.5$, Vo>0	$V_d=V_{sw}$ $=\frac{1}{1-2Dst}Vin$	1 diode 1 switch	4	Two Integrated 2-windings	Input-output isolation. Lower device stress.
Diode/Capacitor assisted Z-source, QZS (Gajanayake et al., 2010),(Gajanayake et al., 2009)	Diode Assisted: $B[(1-Dst)(1-2Dst)]^{-1}$ Where, $0\leq Dst\leq 0.5$, Vo>0	$\frac{1}{1-Dst}Vin$	3 diodes	3	3	Higher voltage boost and lower voltage stress across the capacitor compared to ZSI/qZSI. Number of passive and active components increases with number of stages.
	Capacitor Assisted: $B=[1-3Dst]^{-1}$ Where, $0\leq Ds\leq 0.33$, Vo>0	$\frac{1}{1-3Dst}Vin$	2 diodes	4	3	
Switched Inductor(Miao et al., 2010),(Itozakura and Koizumi, 2011)	$B=(1+D)/[1-3D]^{-1}$ Where, $0\leq D\leq 0.33$, Vo>0	$\frac{(1+D)}{1-3D}Vin$	7 diodes	2	4	Higher voltage boost and lower voltage stress across the capacitor compared to ZSI/qZSI. Number of components increases with corresponding size and cost.
TSTS Z-Source (Long et al., 2013),(Poh Chiang and Blaabjerg, 2013)	Boost: $nb=\frac{2D2-1}{1-D1}$	(2+k)Vin	3 Switches	2	3	Reduced the number of active semiconductors. Buck-boost capability. Common ground. Lower device stress. Higher power density.
	Buck-Boost: $B=1+\frac{1-2D2}{1-D1}$	(1+k)Vin	3 Switches	2	3	

Distributed Z-source(Peng, 2008),(Shuai and Peng, 2011)	Buck :$B=[\sqrt{(2D^2+K)^2+8KD^2}-(2D^2+)]/(2K)$ Where, $0\leq D\leq 1$, and $K=4L_{lk}f_{sw}/R_l$, $Vo>0$ Boost: $B=0.5\sqrt{P^2+4(P/D)}-P$ Where, $0\leq D\leq 1$, and $K=R_l/4L_{lk}f_o$, $Vo>0$	Distributed Impedance	Eliminates discrete active and passive components for impedance network design. High-frequency operation could lead the converter to better transient performance higher power density. Eliminate parasitic effects.

2.4 Summary

As discussed earlier the first publication of “Z-source network” was proposed in 2002 which was a new stage in electric power conversion system to overcome most of the problems faced by traditional converter topologies. The impedance source converter provides a new electric power conversion concept (Peng, 2002; Peng et al., 2003); Since the publication of the first Z-source network, there have been numerous contributions in the literature modifying the basic topology to suit the needs of many applications.

The outstanding performance of z-source network made the researchers and designers curious to explore more about various converter topologies which can apply for different applications. Various comparisons of impedance-source networks are available in the literature based on various specific applications (Miaosen et al., 2007a; Florescu et al., 2010).

There is no common topology or particular circuit which can apply in all applications. However, one may identify niche applications for particular networks that can improve the efficiency, reliability, and power density of the system. The original Z-source network has been advanced to quasi-Z source network, trans-Z-source network, distributed Z-source network, and many other types of Z-source network topologies. The original ZSI has been expanded to DC–DC, DC-AC, AC-DC, and AC-AC converters, respectively, in both two-level and multilevel structures with voltage-fed and current-fed from the power source.

Over one thousand papers have been published and hundreds of Z-source converters have been proposed. In addition, each type (DC-DC, DC-AC, AC-DC, or AC-AC) of converter could potentially be implemented with the original Z-source network, quasi-Z-source network, trans-Z-source, embedded Z-source, semi-Z-source, distributed Z-network, switched inductor Z-source, tapped-inductor Z-source, diode-assisted Z-source, or capacitor-assisted Z-source. The number of combinations is large and the topologies are confusing. Major Z-source network topologies have been investigated and categorized based on conversion functionality and switching configurations.

Chapter 3

Modulation Techniques, Control Methods and THD

3.1 Overview

To have a desirable output voltage and output current along with amplitude, frequency and phase, various control methods and modulation techniques are indispensable to control and modulate the converters. Moreover, all control techniques and pulse width modulation methods by modifying the shoot-through time period to control the Z-source converter are still valid. On the other hand, “in addition to all states in the traditional modulation techniques, a new state called a shoot-through state is introduced and embedded into the modulation strategy for impedance-network based power converters without violating the volt-sec balance in the operating principle”. New pulse width modulation techniques are inspired from sinusoidal SPWM (Fang Zheng et al., 2005b; Miaosen et al., 2004) which by utilizing the distinctive properties of shoot-through state and space-vector modulation (Ali and Kamaraj, 2011a; dos Santos et al., 2010b) are advanced to regulate the output voltage. In addition, various control methods for various applications (Xinping et al., 2007a; Rajaei et al., 2008) will be discussed in detail in a subsequent section.

The literature considered the most applicable control methods and modulation techniques to evaluate the system based on performance and complexity. The

operation principal, network modelling and control techniques of impedance network for electric power convertors can be seen in section (3.2). The classification of different control methods and modulation techniques with diverse switching configuration is discussed in section (3.3). Section (3.4) investigates on harmonic distortion and effects in electrical power systems.

3.2 Operating Principle, Modelling and Control

3.2.1 Operating Principle

An impedance-source network can be generalized as a two-port network with a combination of two basic passive linear elements, e.g. L and C (a dissipative component R is generally omitted). However, different derivations and modifications of the network are possible to improve the performance of the circuit by adding different nonlinear elements in the impedance network, e.g., diodes, switches, and/or a combination of both. The impedance-source network was originally invented to overcome the limitations of the voltage source inverter (VSI) and the current source inverter (CSI) topologies, which are mostly used in electric power conversion (Siwakoti et al., 2015a). Figure (3.1 (a)) shows the principal of operation for three-phase ZSI. In comparison to the conventional three-phase VSI, Z-source inverter has an extra shoot through time period which is feasible by gating-ON of any upper or lower phase legs (Peng, 2002). The basic carrier of pulse width modulation for controlling the shoot-through zero state can be seen in Figure (3.1 (b)).

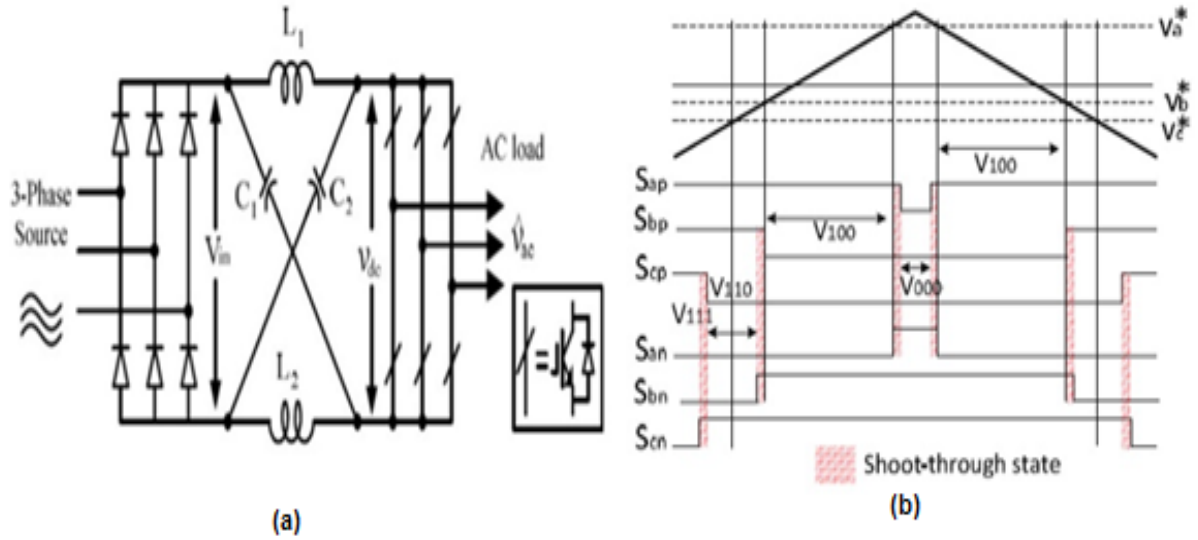


Figure 3.1 Basic impedance network illustrating the operation of a) voltage-fed Z-source inverter with (b) modified carrier-based PWM control with evenly distributed shoot-through states among the three phase legs

In the conventional VSI any shoot-through time period is prohibited as it can short circuit the DC-link. Both Z-source network and shoot-through time period deliver a unique buck-boost feature of the inverter. The peak DC-link voltage ($\hat{v}_{\mathrm{DC}}$) across the inverter bridge is a function of the shoot-through duty cycle ($\hat{v}_{DC} = \mathrm{M}\,[1-2Dst]^{-1}\mathrm{V_{in}}$) so, theoretically, the output voltage of the converter ($\hat{v}_{DC}=\frac{\mathrm{M}\,[1-2\mathrm{Dst}]^{-1}}{2}V_{in}$), where M is the modulation index and D_{st} is the shoot-through duty cycle can be varied to any value from 0 to ∞. However, some practical aspects to the performance of the converter need to be considered for large voltage buck or boost operation, e.g., to avoid exceeding the device limitations, stability, etc.

3.2.2 Modelling and control

The non-minimum phase behaviour of Z-source network because of zero in the right half plane could impose a limitation on the controller design. With the aim of implementing a great control technique, having a good dynamic-model is indispensable .This chapter presents different dynamic models which can be applied for different application with different control techniques and complexity (Poh Chiang et al., 2007d; Yushan et al., 2011). To derive an accurate small-signal model, various state variables are selected, such as the input current (i_{in}(t)), inductor currents($i_{L1}(t), i_{L2}(t), \dots$), capacitor voltages ($v_{C1}(t), v_{C2}(t), \dots$) and load current($i_L(t)$.

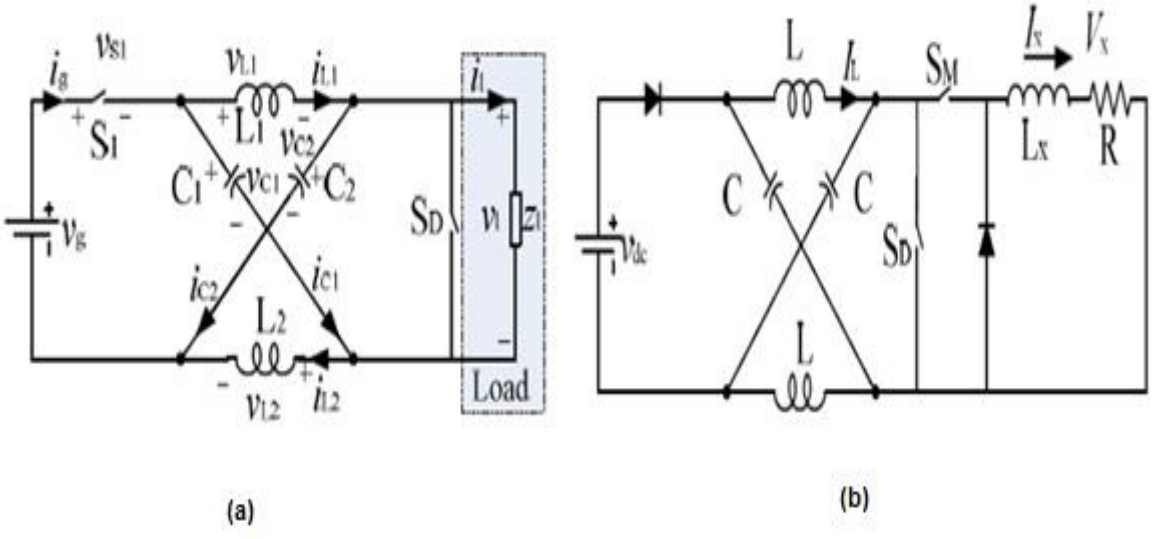


Figure 3.2 Simplified equivalent circuit of Z-source converter for small-signal modelling: (a) D_{st} as control variable and (b) D_{st} and M as control variable

The small-signal model provides the required transfer function for the controller design and provides a detailed view of the system dynamics, helps to understand the system

limits, and provides guidelines for system controller design. In general, M and D_{st} are considered as control variables and the capacitor voltage $(v_c\,(t))$ or the DC-link voltage $(v_{PN}\,(t))$ and the load voltage $(v_x\,(t))$ as variables to be controlled. Figure (3.2 a) shows the simplified Z-source converter model for small-signal analysis, where $(v_c\,(t))$is controlled using D_{st} as a control variable (control switch SD).

This is the most simplified model, however it does not guarantee tight control of $v_x(t)$, which requires an additional control variable M (control switch S_M) as shown in Figure (3.2(b)) (Miaosen et al., 2007b). In addition to the state variables, the parasitic resistance of the inductor (r) and the equivalent series resistance (ESR) of the capacitor (R) have a significant effect on the dynamics of the system and also considered during modelling of the converter to analyse the sensitivity of the circuit under parameter variations (Li and Peng, 2012; Lannert et al., 2013; Gajanayake et al., 2005; Yushan et al., 2011; Gajanayake et al., 2006). Numerous models of small signal with different variable for symmetric/ asymmetric Z-source inverter have been presented in (Poh Chiang et al., 2007d; Galigekere and Kazimierczuk, 2011; Miaosen et al., 2007b) and for quasi-Z-source inverter in (Li and Peng, 2012; Lannert et al., 2013; Qin et al., 2011b; Konga and Gitau, 2012).

Considering the symmetry of the network (using $v_{C1}(t) = v_{C2}(t) = v_C(t)$ and $i_{L1}(t) = i_{L2}(t) = i_L(t)$), a simplified small-signal model is presented in (Poh Chiang et al., 2007d; Xinping et al., 2007a) for ZSI, where the load current is represented by a constant current source. However, such a model describes only the dynamics of the

impedance network and fails to describe the dynamics of the ac load. To overcome this disadvantage, a third-order model is presented in (Miaosen et al., 2007b; Ellabban et al., 2012) using $v_{C1}(t) = v_{C2}(t) = v_C(t)$ and $i_{L1}(t) = i_{L2}(t) = i_L(t)$)and $i_l(t)$ as state variables. In this model, the ac side of the inverter is referred to the DC side with RL load and taking its current as a third state variable.

The dynamic of the system in higher order and modelling of small signal for inverter is proposed in (Feng et al., 2012) and rectifier (Qin et al., 2009b). The complexity in formulating the small signal model and the control-loop design increases with the increase in state variables. To simplify this, various assumptions (symmetry in impedance network, balanced load) and simplifications (representation of AC load/source by its equivalent DC load/source) are prevalent in the literature without losing its generality and change in dynamic performance.

The state-space-averaged small-signal modelling provides a derivation of various control-to-output ($G_{d_0}^{\widehat{v_c}}(s)$) and disturbance-to-output ($G_{v_{in}}^{\widehat{v_c}}(s)$) , ($G_{I_{Load}}^{\widehat{v_c}}(s)$) transfer functions, which helps to predict the system dynamics under the influence of various parameter changes. The root locus of the control-to output transfer function in the S-domain gives a clear map of the converter dynamics. In addition, predicting a Right-Half-Plane (RHP) zero in the control-to-output transfer function is a major advantage of small-signal modelling. The presence of RHP zeroes indicates that the non-minimum phase undershoot (the controlled capacitor voltage dips before it rises in response to a D_{st} increase, generally tends to destabilize the wide-band feedback

loops, implying high gain instability and imposing control limitations. This means that the design of a feedback loop with an adequate phase margin becomes critical when RHP zeroes appear in the transfer function.

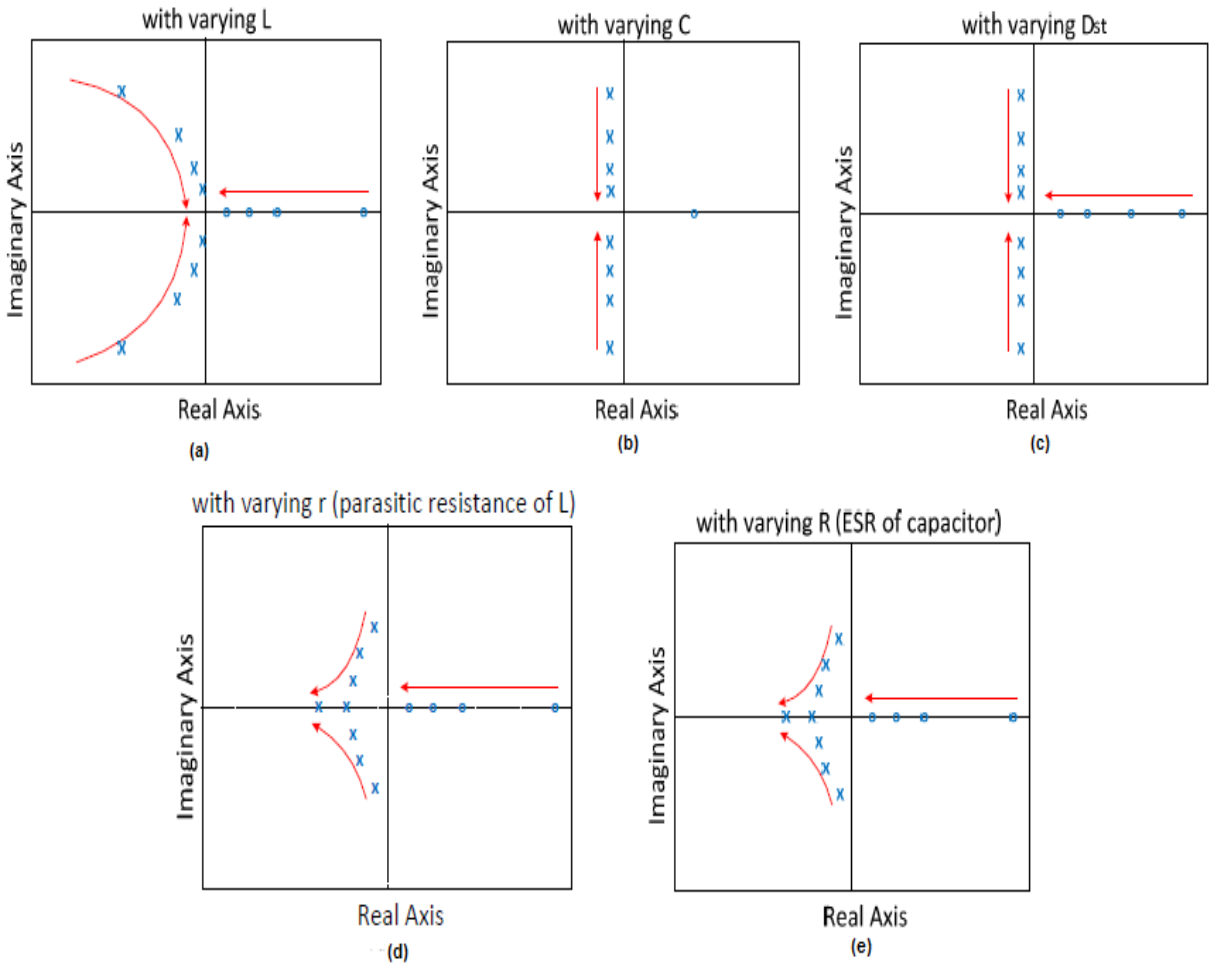


Figure 3.3: Locus of poles and zeroes of control-to-output transfer function with varying (a) inductance (L), (b) capacitance (C), (c) shoot-though duty cycle (Dst), (d) parasitic resistance of inductor (r) and (e) equivalent series resistance (ESR) of capacitor

Various analyses of the pole-zero location and the impact of parameter variations on the converter dynamics are studied considering the wide operating ranges of different sources, e.g., fuel cells and photovoltaic.

The locus of poles and zeroes of control-to-output transfer function by changing inductance (L), capacitance (C), shoot-though duty cycle (D_{st}), parasitic resistance of inductor (r) and equivalent series resistance (ESR) of capacitor (R) can be seen in Figure (3.3).

The parameters variation has an influence on the converters dynamic which categorised in table (3.1).

Table 3.1 summary of impact of parameter variations on the Z-source converter dynamics

Effect on Position of				
Parameter	**Change**	**Conjugate**	**RHP Zeroes**	**Impact on System Dynamics**
Inductance(L)	increasing	Move toward the imaginary axis	Move toward the imaginary axis	Increase non-minimum phase undershoot. Increase settling time. Increase oscillatory response. Decrease natural frequency.
Capacitance (C)	increasing	Move toward the real axis	Constant	Increase system damping. Increase rise time. Increase system settling time. Decrease natural frequency.

Shoot-through duty cycle (D_{st})	increasing	Move toward the real axis	Move toward the imaginary axis	Increase non-minimum phase undershoot. Increase system settling time. Decrease natural frequency.
Equivalent series resistance(ESR) of capacitor(R)	increasing	Move toward the real axis	Move toward the imaginary axis	Increase system damping. Increase non-minimum phase undershoot. Increase current ripple through C
Parasitic resistance of inductor(r)	increasing	Move toward the real axis	Move toward the imaginary axis	Increase system damping. Increase non-minimum phase undershoot. Increase voltage ripple across L.

The effect of varying the parameters on the converter dynamics as mentioned earlier could make a new path for the designer to have a choice on element's values, at the same time considering the limitation of the design, for instance, cost and volume of the elements, ripple content, damping factor, bandwidth control of the feedback, resonant frequency and undershoot or overshoot in the desired output.

Different close loop control techniques studied to control the DC-link voltage and improve the transient response of Z-source inverter (Xinping et al., 2007a; Rajaei et al., 2008) which inspired from the influence of varying parameter and effect of poles and right half plane zeroes. As discussed earlier all control techniques have two control degrees of freedom i.e. shoot through time period (D_{st}) to control the DC-link directly/indirectly, and modulation index (M) to control the output voltage.

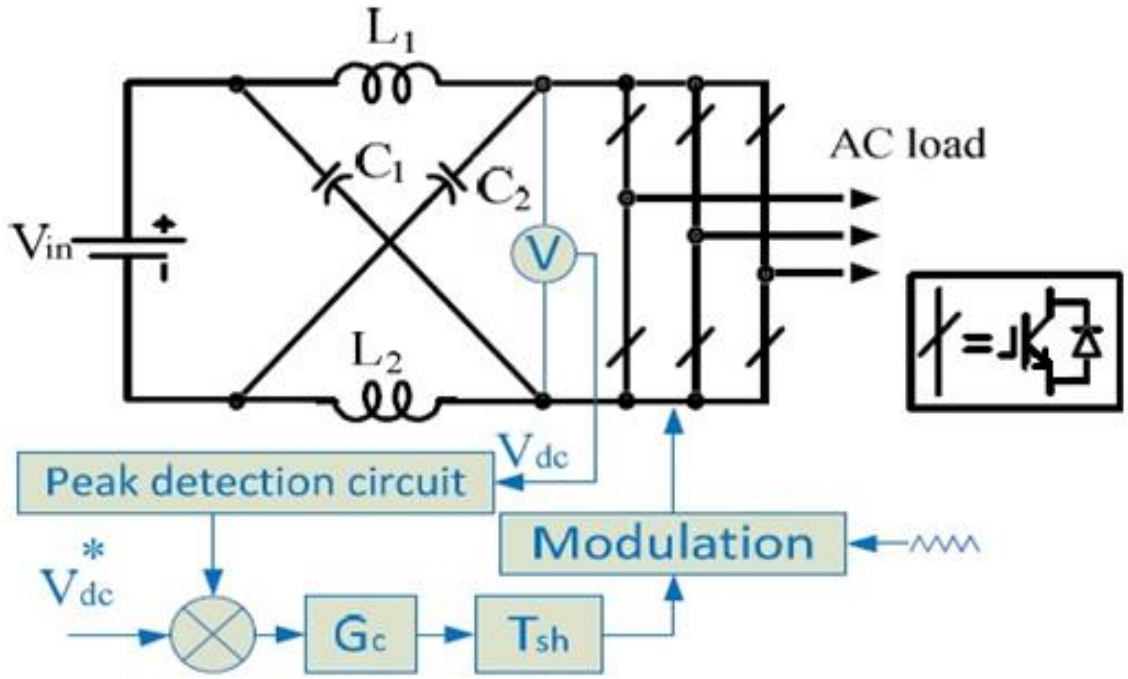


Figure 3.4 Control of DC-link voltage by direct DC-link voltage control

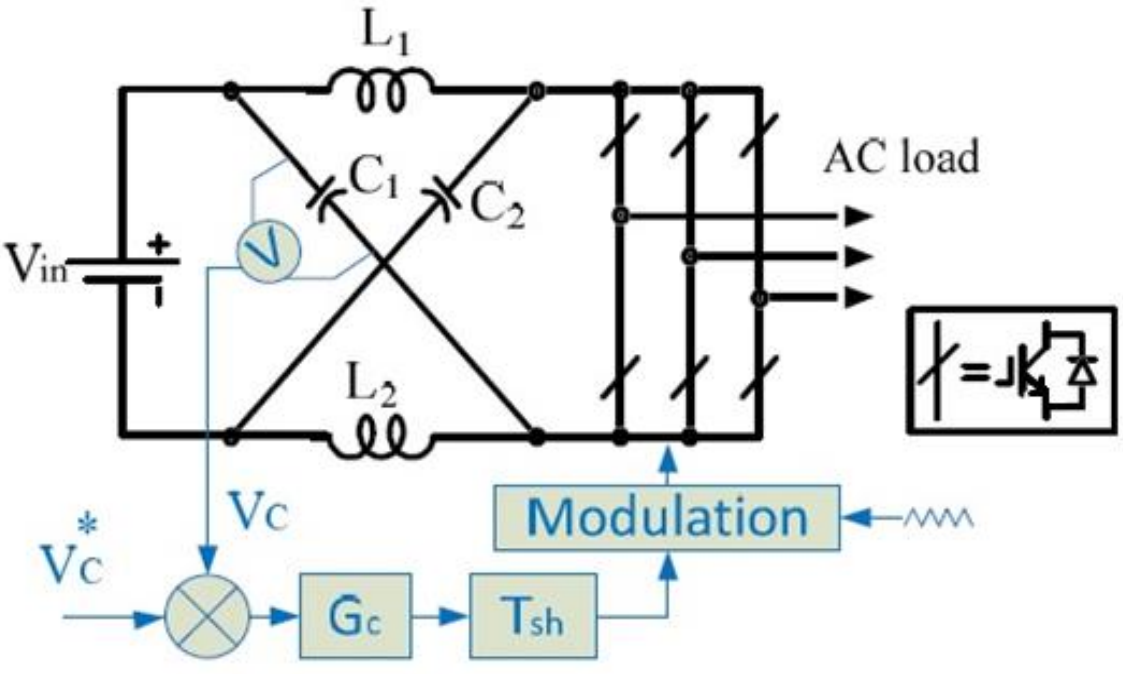


Figure 3.5 Control of DC-link voltage by Capacitor voltage control

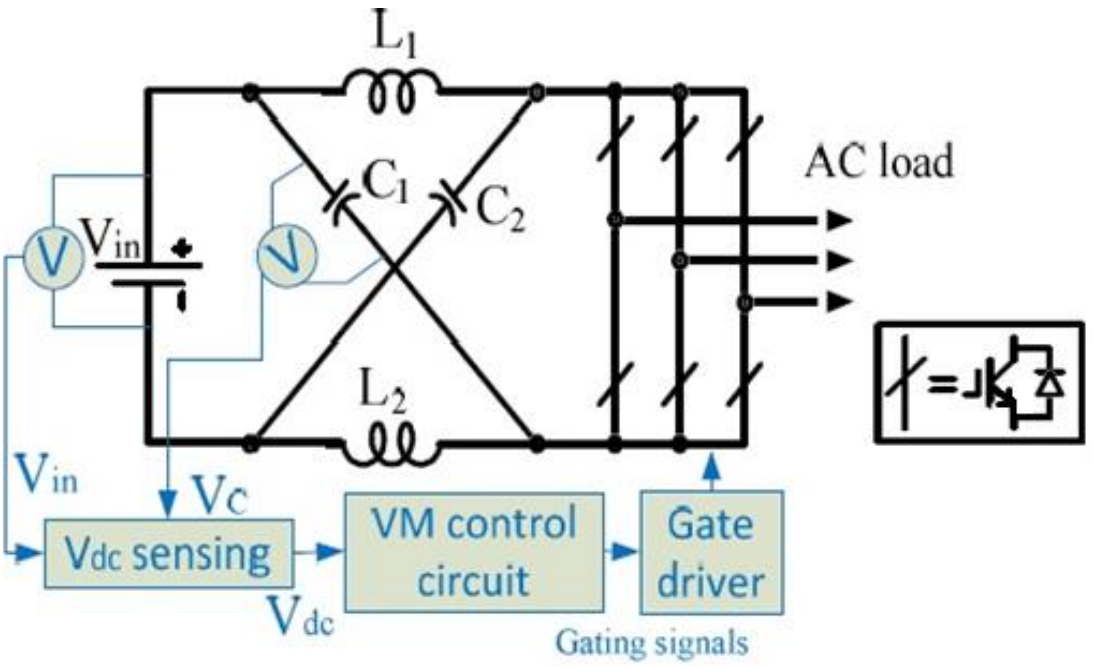


Figure 3.6 Control of DC-link voltage by Voltage mode control (VM)

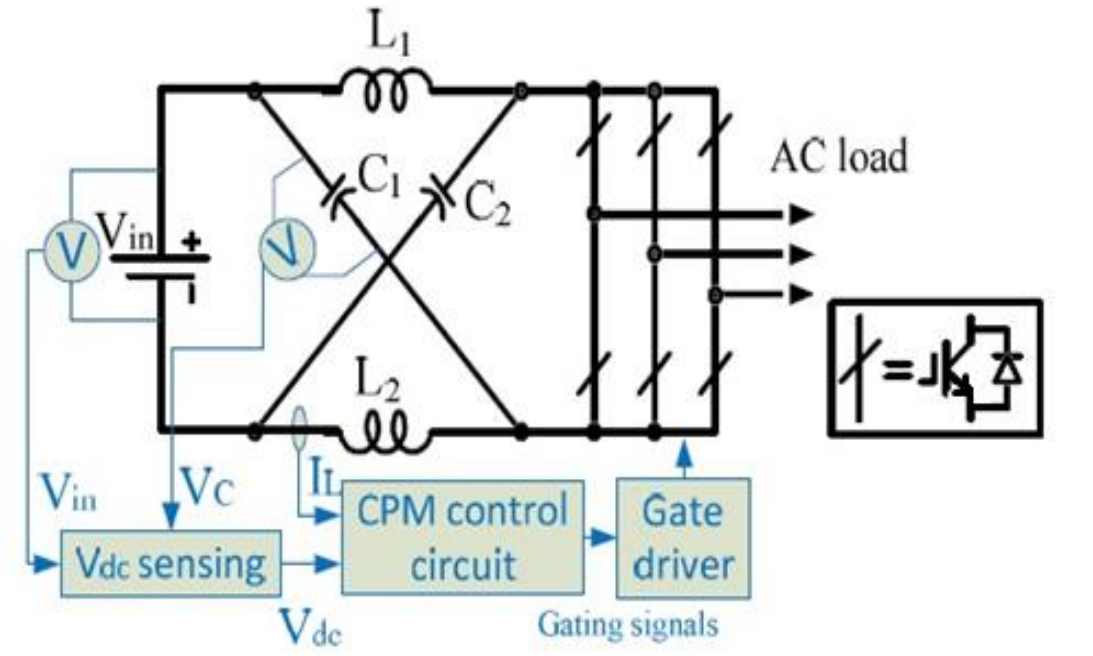
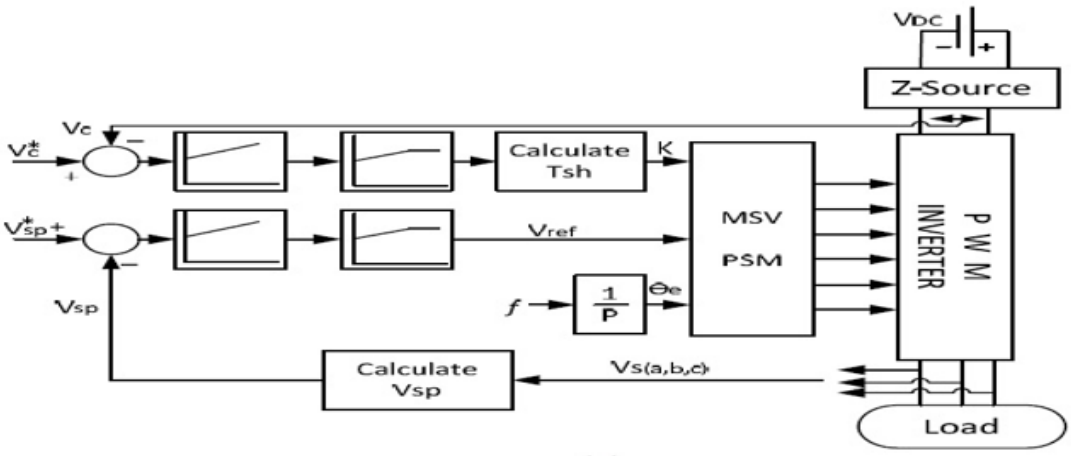


Figure 3.7 Control of DC-link voltage by Current-programmed mode (CPM)

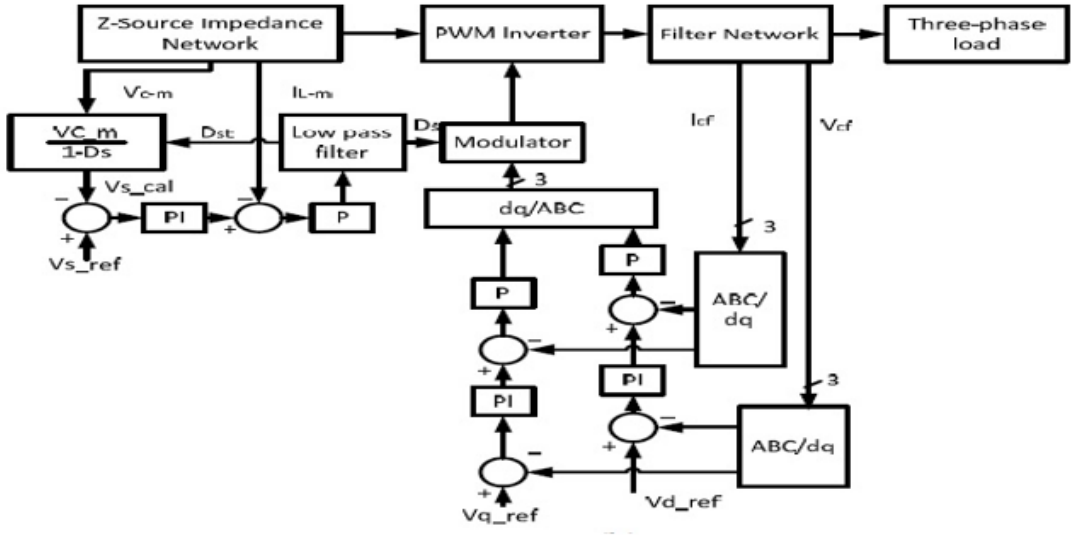
A direct peak DC-link voltage boost control techniques presented in (Xinping et al., 2007b). Figure (3.4) shows the DC-link voltage with specific direct senses and scaling methods and modulation techniques to enhance the transient response, simplifying the controller and reducing the voltage stress. Figure (3.5) shows the voltage of capacitor in indirect strategy that usually captured and compared with desired voltage for measuring the capacitor voltage (V_c) of Z-source inverter (Xinping et al., 2007a; Xinping et al., 2008a) , also predicting the DC-link voltage by measuring the voltage of capacitor and input voltage can be seen in Figure (3.6) and Figure (3.7), (Sen and Elbuluk, 2010).

Changing the input voltage in indirect strategy by modifying the shoot-through time period to control the DC-link is not easy; also, it has an impact on the output voltage as well as changing the modulation index, besides, increasing the switches stress and increasing the harmonic distortion (Xinping et al., 2008a; Sen and Elbuluk, 2010). In the direct strategy by keeping the DC-link voltage constant still complexity of the control method and extra circuit can be seen in the system which this drawback can be solved by predicting the DC-link voltage, calculating the voltage of capacitor and input voltage as shown in Figure (3.6) (VM control method) and Figure (3.7) Current Programmed Mode (CPM), though extra voltage or current sensor is needed. Similar to CPM, a high performance output voltage control using dual-loop peak DC-link voltage control is presented in (Ellabban et al., 2012; Omar Ellabban and D Department, 2011) using digital signal processing (DSP) based on a third-order small-signal model of ZSI.

In comparison with single loop by controlling the voltage of capacitor, in dual loop strategy, by regulating the inductor current in transient state can extend the stability limit of the controller. The indirect strategy has a very simple implementation, but a driver algorithm of the controller will increase the complexity of the design. By controlling the input voltage in feed forward technique with feedback control (Yu et al., 2009a) having a constant peak DC-link with various input voltage is achievable. To find out the shoot-through duty cycle, comparing the input voltage with desired peak DC-link voltage is necessary. In this method the input voltage is compared with the required peak DC-link voltage to calculate D_{st}, and the peak value of output voltage is used to regulate M using a PI controller. A feed forward compensation with bidirectional QZ-source inverter presented in (Feng et al., 2013) to improve the circuit performance with smaller inductance and lower power factor. In the period of non-shoot through duty cycle by rejecting the input voltage disturbance can stabilize the DC-link voltage. Figure (3.8) shows a block diagram of two popular closed-loop voltage control methods of ZSI which consist of both DC-link control and ac output control (Quang-Vinh et al., 2007; Gajanayake et al., 2007; Vilathgamuwa et al., 2009). An example of such control is demonstrated in (Liu and Liu, 2012) for electric vehicle motor drives using a bidirectional Z-source inverter (BZSI) and in (Feng et al., 2013) for connecting a BZSI to the grid during the battery charging/discharging operation mode utilizing a proportional plus resonance controller.



(a)



(b)

Figure 3.8 Indirect DC-link voltage controller modules with two degrees of freedom: (a) controller for both DC boost and AC output voltage of Z-source inverter (Jong-Hyoung et al., 2010) and (b) multi loop closed loop controller (Vilathgamuwa et al., 2009)

In these control strategies by modifying the shoot-through state (D_{st}) can control the voltage of the capacitor also with modifying modulation index can control the output

voltage utilizing distinct proportional/ proportional-integrator (P/PI) controller. However, both control parameters are dependent on each other, as change in one parameter imposes a limitation of the changeability of the other due to the insertion of a shoot-through time inside the null period. Putting a maximum limit on the control variable could mitigate this limitation. A hybrid controller using a neural network is implemented in (Rostami and Khaburi, 2010), where model predictive control is used to determine the neural-network plant model. The neural-network controllers are trained offline and then used to predict the system response. This method improves the system response, however at the cost of increasing complexity.

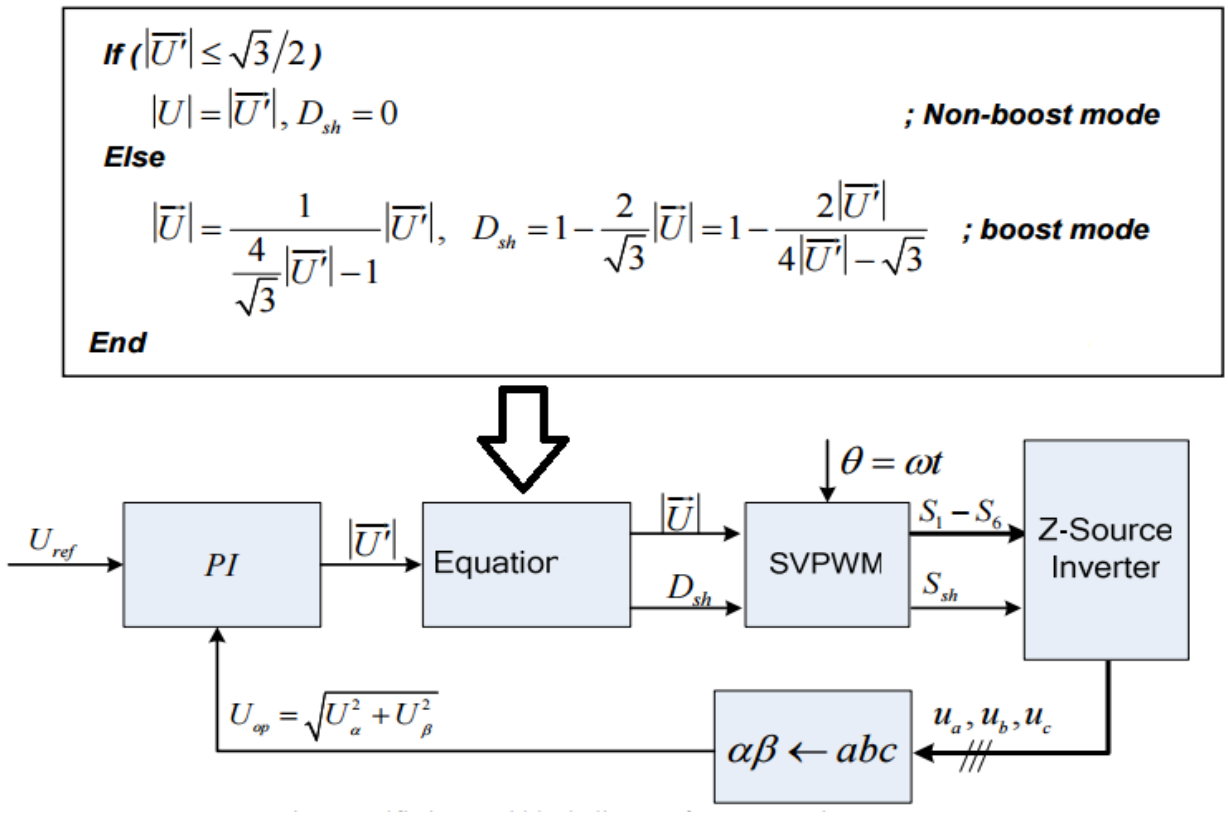


Figure 3.9 Unified control block diagram for the Z-source inverter with one control variable (Shuitao et al., 2008)

To keep enough voltage control margin, the shoot-through duty ratio D_{st} must be less than $1 - \mathrm{M}$ or ($M < 1 - D_{st}$) for the simple boost, which leads to a lower utilization of the input DC voltage and a higher voltage stress across the switches. To address this issue, a unified control technique is presented in (Shuitao et al., 2008) (see Figure (3.9) with only one control degree of freedom ($M \; or \; D_{st}$).

The AC output voltage of the inverter is controlled by keeping the capacitor voltage as a variable. This control method is simple and easy to implement with only one sensor. Similar control strategies are retrofitted to various applications, e.g. grid-connected photovoltaic (Yushan et al., 2013; Jong-Hyoung et al., 2010) distributed generation (Yuan et al., 2013; Vilathgamuwa et al., 2009), and single-phase uninterruptible power supply (Zhi Jian et al., 2008).

The model predictive control (MPC) method proposed by Mo et al.,(2011) has an excellent capability of multi system variable to regulate the load current and voltage as well as impedance network inductor current, also stabilizing the switching frequency along with capacitor voltage. In addition in this method using any controller such as PI or proportional-integral-derivative (PID) or modulation techniques is not necessary. It provides a quick reference tracking capability with a simple feedback control method and can help to reduce the non-minimum phase effect during the transient process. The MPC method to control a Z-source network along with its flow chart are shown in Figure (3.10). Z-source variables (X_k) i.e. load voltage/current is calculated according to this method, also evaluating the discrete MPC system is done by feedback. By

expressing the cost functions can choose the MPC value that is similar to the references values, Hence, the Z-source converter can be implemented by generating the corresponding switching signals (S_K).

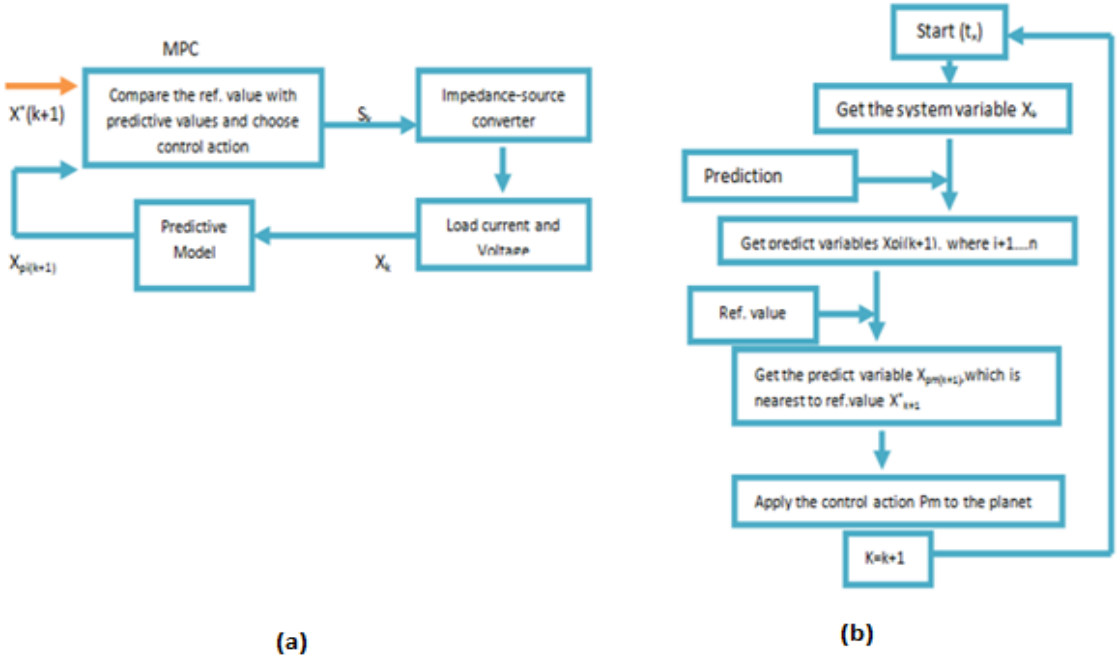


Figure 3.10 Implementation of (a) Model predictive control to impedance-source network with (b) Corresponding flowchart(Rostami and Khaburi, 2010)

By using this strategy can restrain the Z-source network's resonance and input surge current to prevent any damages on the switches. New sliding mode fixed frequency control method for controlling the shoot-through duty ratio and modulation index is proposed in (Jianfeng et al., 2013; Rajaei et al., 2008) for Z-source and quasi-Z-source inverter.

Table 3.2 summary of various control methods for electric power conversion system

References	Control method	Sense signal	Controller type	Mathematical model	Control variable	features
(Miaosen et al., 2007b)	Indirect	V_c and $V_{o(a,b,c)}$	Single-loop nonlinear(gain scheduling+ state feedback)control	State-space averaged small-signal model $X(t)=[v_c i_L i]'$	D_{ST} and M	Controller is very stable in steady state operation. Not suitable for rapidly varying reference point. Complex control algorithm.
(Xinping et al., 2007a)	Indirect	Vc	Single-loop using PID controller	State-space averaged small-signal model $X(t)=[v_{c1} v_{c2} i_{L1} i_{L2}]'$	D_{ST}	Modified simple boost control is implemented. Consider dynamic of impedance network only.
(Xinping et al., 2008a)	Direct	$V_{DC\text{-}link}$	Single-loop using PID-like fuzzy controller	State-space averaged small-signal model $X(t)=[v_{c1} v_{c2} i_{L1} i_{L2}]'$	D_{ST}	Modified simple boost control is implemented. Improved transient response. Enhances disturbance rejection. Simplifies controller design.

(Ellabban et al., 2012) (Sen and Elbuluk, 2010)	indirect	VM mode:v_c and v_{in}	Single-loop using PID Controller	State-space averaged small-signal model $X(t)=[v_{c1}v_{c2}i_{L1}i_{L2}]'$	D_{ST}	Estimate $v_{DC-link}$ by measuring v_c and v_{in}. Good input and load disturbance rejection. Order of system in reduced by one in CPM, which increases the phases the phase margin and offers simple compensator design.
		CPM mode: vc,vin And iL	Dual-loop with PI controller			
(Omar Ellabban and D Department, 2011) (Omar Ellabban, 2011)	Indirect	V_c,v_{in} and i_L	Dual-loop with PI controller	State-space averaged small-signal model $x(t)=[v_c i_L i_l]'$	D_{ST}	Dual-loop capacitor voltage control achieves better steady and transient performance and stability compared to single-loop control. Enhances disturbance rejection.
(Yu et al., 2009a)	Indirect	v_{in} and v_o	Single-loop PI controller with saturation	NA	D_{ST}	Simple and easy to implement. Performs rough regulation. Did not consider the impact of impedance network (RHP pole etc.) in stability.

(Feng et al., 2013)	Direct	$V_{DC\text{-}link}$	Single-loop using PID controller	State-space averaged small-signal model $x(t)=[v_{c1}v_{c2}i_{L1}i_{L2}]'$	D_{ST}	Modified simple boost control is implemented. Improves transient response. Enhances disturbance rejection. Simplifies controller design.
(Quang-Vinh et al., 2007) (Rostami and Khaburi, 2010)	Indirect	v_c and $v_{o(a,b,c)}$	Single-loop using PI controller	NA	D_{ST}	Capacitor voltage is linearly controlled by K=vc/vin. Enhances disturbance rejection from load and input variations.
(Gajanayake et al., 2006) (Gajanayake et al., 2007)	Indirect	V_c,i_L,$v_{cf(a,b,c)}$ and $i_{cf(a,b,c)}$	Multi-loop control with P for inner current and PI for outer voltage loop	State-space averaged small-signal model $x(t)=[v_{c1}v_{c2}i_{L1}i_{L2}]'$	D_{ST} and M	Mitigate transfer of DC-side disturbance to ac side. Excellent reference tracking and rejection of disturbances arising from both input and output sides.
(Shuitao et al., 2008)	Indirect	vo (a , b , c)	Unified control	NA	D_{ST} or M	One degree of freedom Linear control of output voltage using unified voltage vector Low cost and ease of digital implementation

(Shuitao et al., 2008)	indirect	v_{in} , i_{in} , $v_{o\,(a\,,\,b\,,\,c\,)}$ and $i_{o\,(a\,,\,b\,,\,c\,)}$	Single-loop using PI controller	State-space averaged small signal model $x(t)=[v_{c1}v_{c2}i_{L1}i_{L2}]'$	D_{ST}	Battery-assisted qZSI control which controls the state of charge (SOC) of the battery and the power injected into the grid
(Mo et al., 2011) (Mosa et al., 2013)	Indirect	$V_{0(a,b,c)}$ or $i_{o\,(a,b,c)}$	Model predictive control (MPC)	NA	Switching state vector(S)	Quick reference tracking capability Offers multi-system variable regulation considering different system constraints. Suppresses inrush current and resonance in the impedance network
(Jianfeng et al., 2013) (Jianfeng et al., 2011) (Rajaei et al., 2008)	Indirect	Vin,iin,vo(a,b,c)	Sliding mode(Krein et al.) control	Large-signal model $x(t)=[iL1iL2vc1vc2ib]'$	DST and M	Controller designed from large-signal model of Converter. Stable and robust to large parameter, line and load variations. Fast response, less current ripple when subject to large load/source variations. Complex control algorithm

Inspired by the conventional variable-frequency sliding-mode (SM) control, a fixed-frequency sliding-mode control is also presented in (Jianfeng et al., 2013; Rajaei et al., 2008) for ZSI and QZSI to control M and D_{st}. The SM controller is stable and robust to large parameter, line, and load variations as it is designed from a large-signal model of the converter whereas to conventional current- and voltage mode controllers are designed based on linearized small-signal models. This feature of the SM controller has its best niche in applications where a widely varying load and source are connected to the impedance-source converter, e.g., intermittent sources such as PV or fuel cells connected to widely varying loads. Table (3.2) summarizes various control methods with its control variables and features.

3.3 General Classification of Modulation Techniques

The best modulation techniques to maximize the boost, minimize the harmonic distortion, reduce the switches stress and reduce the number of device commutations in each switching period can be achieved by amalgamation of conventional switching concept along with selective shoot-through state. Figure (3.11) shows vast classified impedance-source-network based electric power conversion system using different switching configuration. A combination of various strategies with impedance source inverter provides extensive electric power conversion topologies from medium voltage/current to high voltage/current. Hence, utilizing this switching configuration for unidirectional/bidirectional, isolated/non-isolated converters can employ for any sort of converters (AC-AC), (DC-DC), inverter (DC-AC), and rectifier (AC-DC).

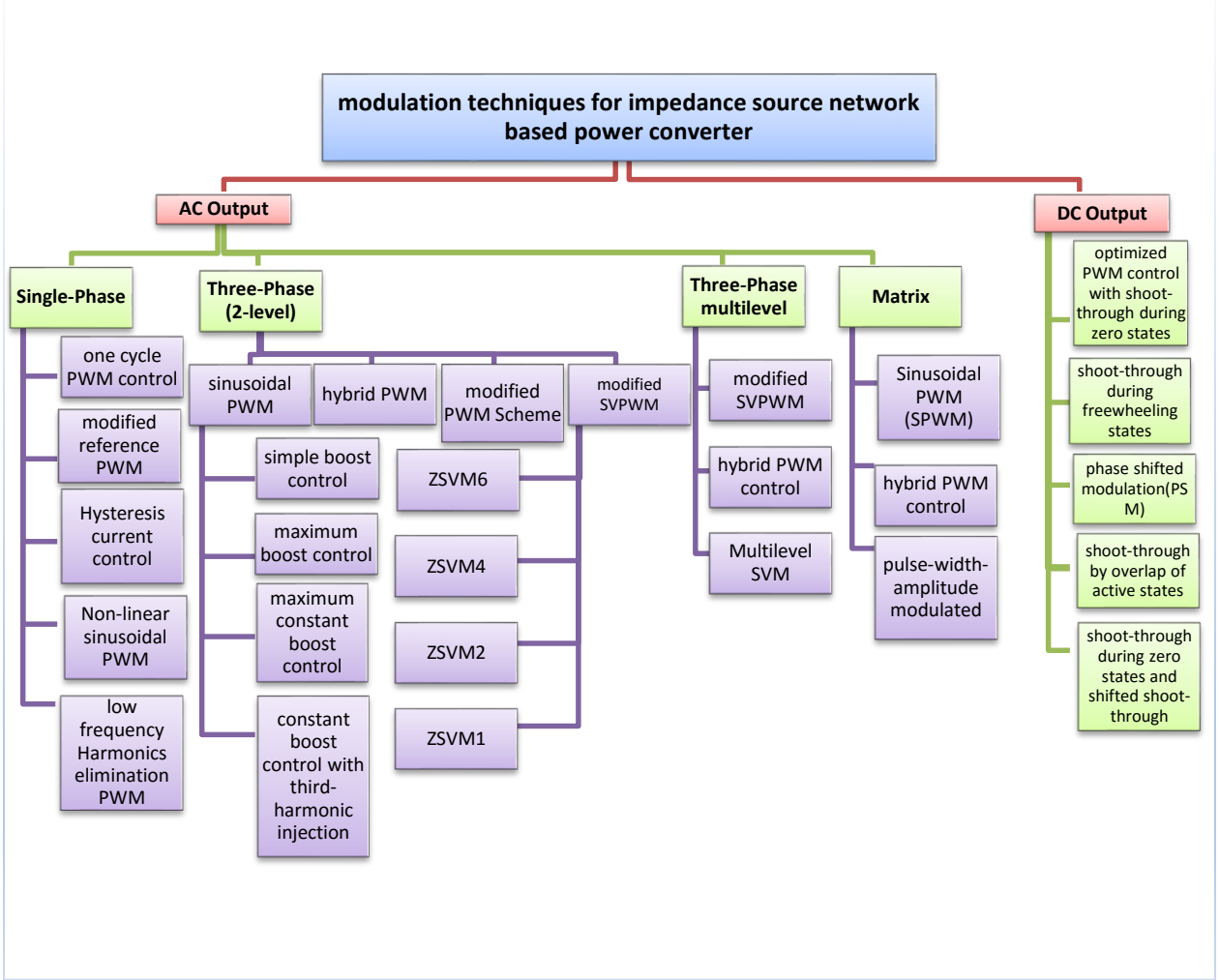


Figure 3.11 Categorization of modulation techniques for impedance-source network-based power converter (Siwakoti et al., 2015b)

3.3.1 Modulation techniques for single phase topologies

Various modulation techniques are presented in the literature to modulate and control the output voltage of single-phase impedance source inverters having two switches for semi Z-source and quasi-Z-source (Dong et al., 2011a; Yu et al., 2011b), 4switches intermediate H-bridge topologies (Dong et al., 2011a; Poh Chiang et al., 2005; Zare and Firouzjaee, 2007), or embedded Z-source (Dong et al., 2011a; Oh et al., 2013) for various application. A two-switch topology offers a simple and cost-effective solution

for a single-phase grid-connected photovoltaic system. Two modulation techniques are prevalent in the literature to control and modulate the two switches of a single-phase Z-source/quasi-Z-source to get the required output voltage, namely one-cycle control (Yu et al., 2011b) and non-linear Sinusoidal Pulse-Width Modulation (SPWM) (Dong et al., 2011a).

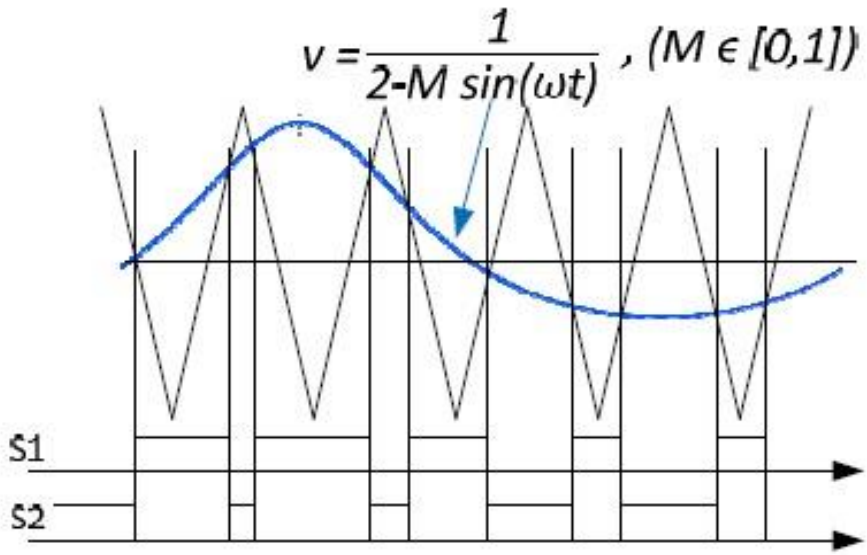


Figure 3.12 Generation of switching signal for 1-ph Z-source inverter using nonlinear sinusoidal pulse width modulation (SPWM)

In semi Z-source/ quasi-Z-source converters, to provide switch drive signal, comparing the non-linear sinusoidal references signal $v = [2 - Msin\,\omega t]^{-1}$ with carrier signal is necessary as shown in Figure (3.12). Comparable modulation strategy called single phase embedded z-source inverter with four switches is presented in (Oh et al., 2013). A one-cycle control method is adopted to control a single-phase semi-Z-source topology in (Yu et al., 2011b). In this control method, two switches work in a

complementary fashion, where the clock signal (CLK) is used to turn ON any one switch. The integrated voltage across the switches can turn the switch gate ON and as the voltage reach to signal $(v_i - v_{ref})$, the integrator will turn OFF the switch as shown in Figure (3.13).

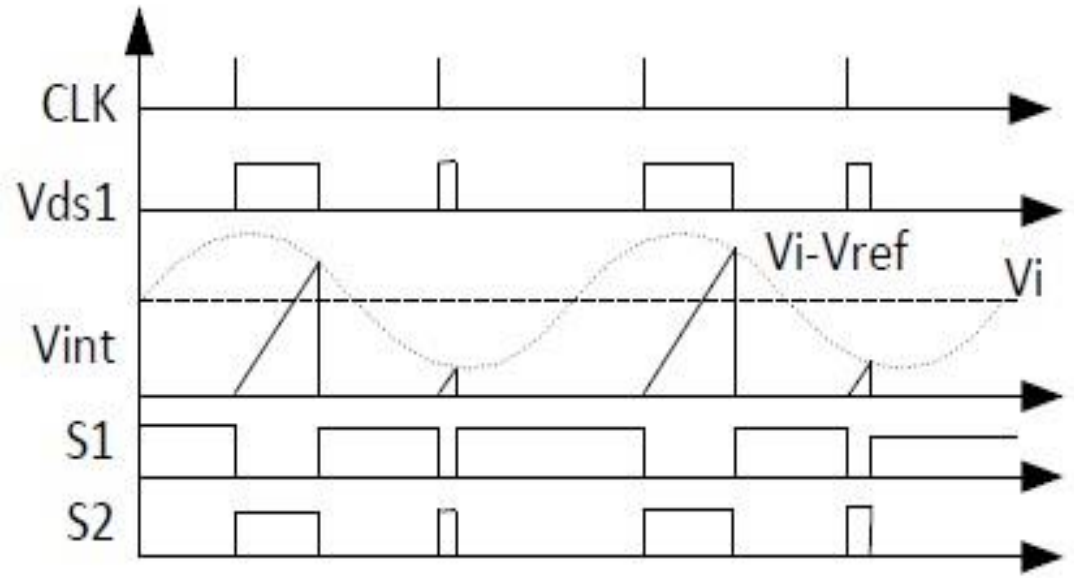


Figure 3.13: Generation of switching signal for 1-ph Z-source inverter using one cycle control method

This control method has the ability to reject input perturbations and is insensitive to the system model, which provides a high-efficiency constant-frequency control. A standard carrier-based PWM is modified in (Poh Chiang et al., 2005) for a single-phase H-bridge topology. Without altering the volt-sec average voltage, a shoot-through duty cycle is located instead of null state as shown in Figure (3.14).

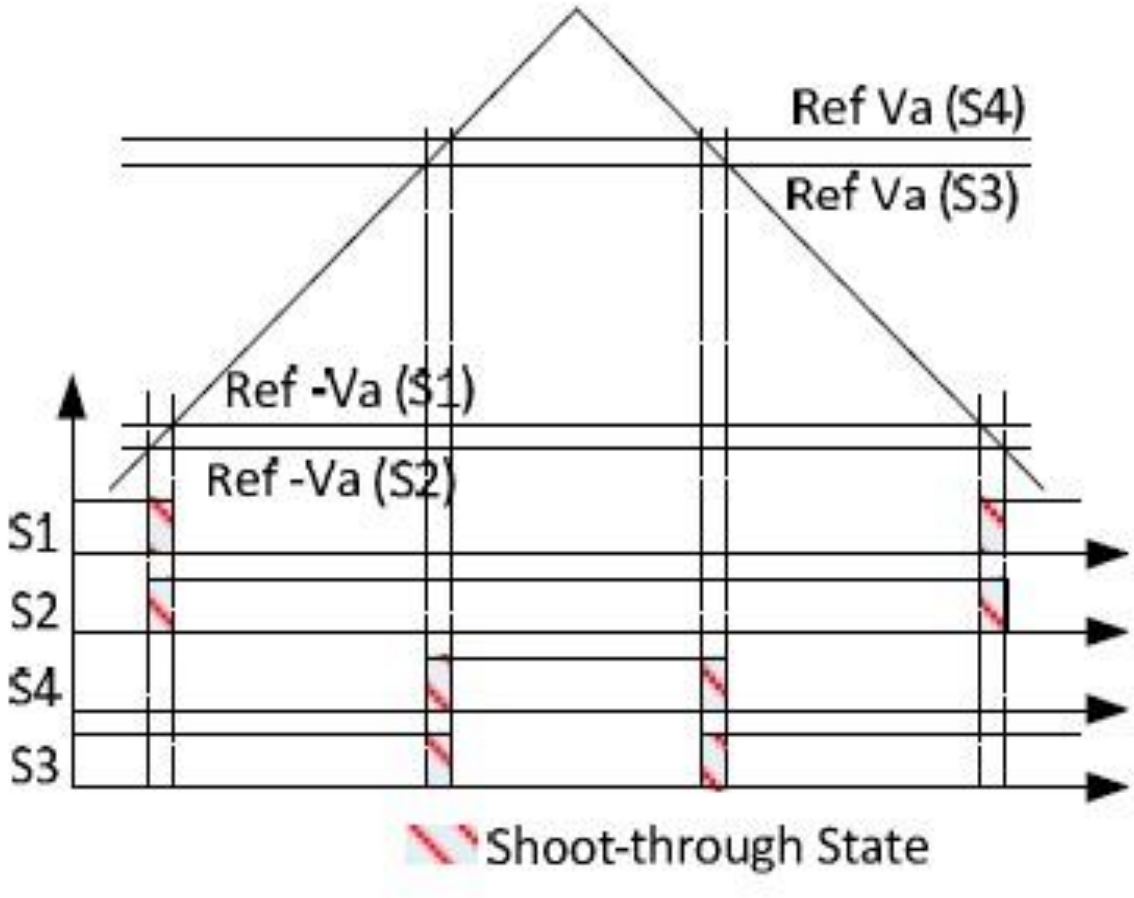


Figure 3.14 Generation of switching signal for 1-ph Z-source inverter using modified space vector modulation SVM

Active state in each switching cycle is kept the same as conventional sinusoidal SPWM. Therefore, the output waveforms are still sinusoidal; however, they are boosted to the desired level by properly controlling the shoot-through time period. Modulation index is extended to the three-phase/four-phase H-bridge topologies for a voltage fed impedance network in both continuous and discontinuous mode.

Table 3.3 comparisons of various modulation techniques for single-phase topologies

Modulation technique	Switching Topology	No. Of Switches	Peak Stress on Switching Devices	Modulating Signal	Range of M and D_{ST}	Features
Nonlinear SPWM	Semi Z-source	2	$V_{SW}=3V_{in}$ $I_{SW}=3I_{in}$	One quasi-sinusoidal modulating signal $v=[2-M\sin \omega t]^{-1}$	$0\le M\le 1$ and $0\le D\le 1$	Eliminate leakage current. Cost-effective solution compared to H-bridge. High device stress. Limited to two switch impedance network topologies.
One-cycle	Single-phase	2	$V_{SW}=3V_{in}$ $I_{SW}=3I_{in}$	One sinusoidal modulating signal (Vin-vref), where vref=Vm sin ωt	$1/3\le D\le 1$	Constant frequency control can be achieved does not need an accurate model of the converter. High device stress. Limited to two switch impedance network topologies. Modulation technique can be extended to N-phase inventers.
Carrier-based PWM	2-leg H-bridge	4	$V_{SW}=BV_{in}$, $I_{SW}=B_{io}$ where $B=[1-2Dst]^{-1}$	Two sinusoidal modulating signals v=M cos ωt for second leg	$0\le M\le 1$ and $0\le Dst\le 0.5$	Modulation technique can be extended to N-phase inverter.

Hysteresis-Band current control	2-leg H-bridge	4	$V_{SW}=BV_{in}$, $I_{SW}=B_{io}$ where $B=[1-2Dst]^{-1}$	A Band of sinusoidal modulating signals $v_{ref}=V_m \sin_{\omega t}$	$0 \leq Dst \leq 0.5$	Suitable for symmetric or asymmetric network topologies. Pure sinusoidal output current. Simple, robust and insensitive to load parameter change. On-uniform switching leads to higher device stress. Switching frequency is not regular.

Furthermore a hysteresis band current system for H-bridge is presented in (Zare and Firouzjaee, 2007) for H-bridge. The performance is tested for both symmetrical and asymmetrical Z-source networks. Similar to the modulation technique used in (Miaosen et al., 2006; Miaosen et al., 2004) for a three-phase inverter, a low frequency harmonics elimination PWM strategy is presented in (Yifan et al., 2011) which has a unique feature of reducing the output harmonic distortion, size and cost of the system. Furthermore, a modified Z-source using two switches is proposed in (Boldea et al., 2008) which reduced the cost of the circuit. These modulation methods reviewed for single-phase impedance network-based converters, is summarized in Table (3.3).

3.3.2 Modulation Techniques for Three-Phase Topologies (2-level)

Different pulse width modulation methods with the purpose of reducing the commutation times, less voltage stress and easy implementation are discussed in this chapter. Two level modulation techniques are largely classified as sinusoidal SPWM and Space Vector Pulse Width Modulation (SVPWM). different modification including simple boost, maximum boost and maximum constant boost as well as constant boost with 3rd harmonic injection are presented in (Fang Zheng et al., 2005b; Yuan et al., 2009).

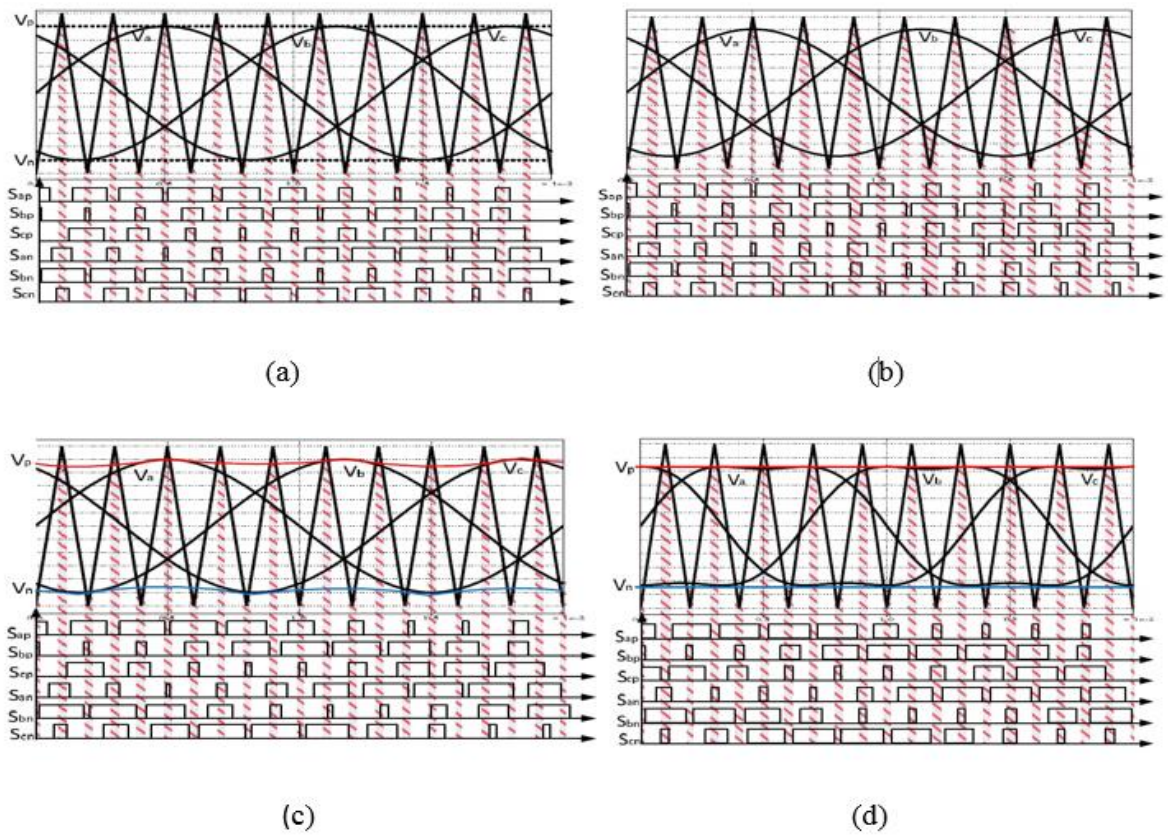


Figure 3.15 Sine wave PWM (a) simple boost control, (b) maximum-boost control, (c) maximum-constant-boost control, and (d) constant-boost control with 1/6th of third harmonic injection (→Shoot-through period)(Rostami and Khaburi, 2009)

Various control techniques of SVPWM for voltage gain comparison have been presented in (Rostami and Khaburi, 2009). Simple boost control is the most basic and is derived from the traditional sinusoidal SPWM where a carrier triangular signal is compared to the three-phase reference signal for sinusoidal output voltage and two straight lines (V_p and V_n) to create shoot-through for voltage boost as shown in Figure (3.15(a)). However, by decreasing the modulation index, shoot-through time period increases simultaneously. The main drawback of this modulation technique is the shoot-through time period which restricted to $D_{st,max} = (1 - M)$ and boost factor limited to $B = [2M - 1]^{-1}$.

Another drawback of this modulation technique, increasing the device stress when a greater voltage boost is needed. To overcome this problem, maximum boost pulse width modulation control technique is proposed in (Fang Zheng et al., 2005b). The maximum boost modulation techniques retain six active states as same as conventional carrier control and uses all zeroes to create shoot-through time period as shown in Figure (3.15(b)). By turning all zeroes to shoot-through time period, boost factor increases to $B = \pi [3\sqrt{3} - \pi]^{-1}$, Hence, reducing the devices stress in comparison with simple boost control system. Due to the variation of shoot-through time period, low frequency harmonics in the passive component can increase the cost and volume of the circuit. By eliminating the low frequency surge in the impedance-source network components, can have the maximal boost factor along with constant shoot-through time period.

A maximum constant boost control techniques is presented in (Miaosen et al., 2006; Miaosen et al., 2004). Maximum-constant-boost waveform can be seen in Figure (3.15(c)). By 3rd harmonic injection can increase the range of modulation index from 1 to $\frac{2}{\sqrt{3}}$, also by utilizing two straight lines (V_p, V_n) can produce the shoot-through state as shown in Figure (3.15(d)). Comparison of maximum-constant-boost method with other sine PWM techniques is shown in Table (3.4).

Table 3.4 Comparisons of various SPWM techniques in three-phase z-source bridge inverters

Parameters	Simple boost	Maximum boost	Maximum boost with third harmonic Injection	Maximum constant boost	Maximum constant boost with third harmonic Injection
$\bar{T}_0/T$	1-M	$\frac{(2\pi - 3\sqrt{3M})}{2\pi}$	$\frac{(2\pi - 3\sqrt{3M})}{2\pi}$	$1-\frac{\sqrt{3}}{2}M$	$1-\frac{\sqrt{3}}{2}M$
Boost Factor (B)	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3M}-\pi}$	$\frac{\pi}{3\sqrt{3M}-\pi}$	$\frac{1}{\sqrt{3M}-1}$	$\frac{1}{\sqrt{3M}-1}$
Voltage Gain(G)	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3M}-\pi}$	$\frac{\pi M}{3\sqrt{3M}-\pi}$	$\frac{M}{\sqrt{3M}-1}$	$\frac{M}{\sqrt{3M}-1}$
Voltage Stress of the Switch	$(2G-1)V_o$	$\frac{3\sqrt{3G}-\pi}{\pi}Vo$	$\frac{3\sqrt{3G}-\pi}{\pi}Vo$	$(\sqrt{3G}-1)Vo$	$(\sqrt{3G}-1)Vo$
Maximum(M)	1	1	$2/\sqrt{3}$	1	$2/\sqrt{3}$

Similar to the SPWM techniques, SVPWM also helps to reduce the device commutation, harmonic distortion, voltage stress and losses in switches.

The unique feature of this technique is to utilize the SVPWM in different Z-source inverters. Inserting the shoot-through time period in the switching period with no

alteration for volt-sec is vital to decrease the device commutation and losses in the switches. The literature includes different SVPWM methods such as: ZSVM2 (Ali and Kamaraj, 2011a), ZSVM4 (Jin-Woo and Keyhani, 2007) and ZSVM6 (Yushan et al., 2011). A comparison of various SVM techniques is shown in Table (3.5) and presented in (Yushan et al., 2014a; Liu et al., 2013a), experimentally based on various performance analyses along with two new modifications, i.e. ZSVM1-I and ZSVM1-II. Modified SVPWM techniques are also being used to reduce the common mode voltage and leakage currents for photovoltaic systems (Siwakoti and Town, 2012; Bradaschia et al., 2011) and motor derives (Siwakoti and Town, 2013).

Table 3.5 Comparisons of various SVM techniques in three-phase bridge inverters

Parameters	ZSVM1	ZSVM2	ZSVM4	ZSVM6
D_{max}	$(1-\frac{3\sqrt{3}M}{2\pi})/2$	$(1-\frac{3\sqrt{3}M}{2\pi})$	$3(1-\frac{3\sqrt{3}M}{2\pi})/4$	$(1-\frac{3\sqrt{3}M}{2\pi})$
B_{max}	$2\pi/(3\sqrt{3}M)$	$\pi/(3\sqrt{3}M-\pi)$	$4\pi/(9\sqrt{3}M-2\pi)$	$\pi/(3\sqrt{3}M-\pi)$
G_{max}	$2\pi/(3\sqrt{3})$	$\pi M/(3\sqrt{3}M-\pi)$	$4\pi M/(9\sqrt{3}M-2\pi)$	$\pi M/(3\sqrt{3}M-\pi)$
Voltage Stress of the Switch,(Vs)	$\left(\frac{2\pi}{3\sqrt{3}M}\right)$Vin	$\left(\frac{3\sqrt{3}G}{\pi}-1\right)$Vin	$\left(\frac{9\sqrt{3}G}{2\pi}-2\right)$Vin	$\left(\frac{3\sqrt{3}G}{\pi}-1\right)$Vin
No. Of shoot-through per switching cycle	2	4	6	6
Current ripple in the inductor(ΔI_L)	Highest	Medium	Low	lowest

The hybrid PWM technique (dos Santos et al., 2010b) is the combination of the theory of SVPWM with triangular-comparison pulse width modulation which decreases the algorithm-calculation of the system. Also, three phase four wire converter with Hybrid-PWM techniques is presented in (dos Santos et al., 2010a). Based on one-cycle control, a control technique as shown in Figure (3.13) for three-phase Z-source/quasi-Z-source is presented in (Gajanayake et al., 2009). This is complemented by a random PWM scheme proposed in (Gao et al., 2006) for a Z-source inverter whose purpose is to reduce common mode voltage when used in an AC motor drive. For current fed QZSI, (Qin et al., 2014) also proposes a modified SVPWM scheme for achieving higher input current utilization, lower switching loss, lower total harmonic distortion and lower switching spikes across switching devices compared to traditional SVPWM (dos Santos et al., 2010b; Qin et al., 2009a). These advantages are attributed to the full-wave symmetrical modulation (FSM) applied whose outcome is only one short zero state vector $(\vec{I}\,7, \vec{I}\,8, \vec{I}9)$ utilised in each switching period.

3.3.3 Modulation techniques for three-phase multilevel topologies

Neutral point clamped PWM inspired from conventional SVPWM utilizing 2-D victorial representations along with “origin shifting”. However, correct integration of the shoot through state sequence with the classical PWM is essential for proper Z-source NPC operation, as some of the vectors can cause a short circuit across the full DC-link which then results in zero voltage output. Keeping the volt-sec balanced is significantly vital so long as sequencing of D_{st} to precisely provide the required three-phase

sinusoidal output voltage. Proper amalgamation of D_{st} with classical PWM is necessary to attain maximum voltage boost, reduced total harmonic distortion, less voltage stress as well as minimum commutation times.

Control of the Z-Source NPC with continues/discontinues modulation method along with two Z-source networks is presented in (Poh Chiang et al., 2007a) which previously was introduced as continues Edge-Insertion and continues Modified-Reference with minimum commutation time; lately introduced as traditional 60^0 discontinue and origin-shifted-60^0-discontinuous pulse width modulation technique. The device commutation count with EI-PWM is maximum eight, which reduces to six with the continuous modified reference technique.

The number further reduces to a minimum of four with the discontinuous PWM technique is opted for. However with the same shoot-through duty ratio, the reduced number of shoot-through per switching cycle in the discontinuous scheme will produce lower common-mode voltage but higher inductor current ripples which significantly increase the size of the passive component in the impedance network. A detail comparison of continuous and discontinuous PWM schemes is provided in (Poh Chiang et al., 2007a). A nearest-three-vector (NTV) modulation principle and reduced common-mode (RCM) switching is proposed in (Poh Chiang et al., 2007b) to minimize harmonic distortion, device commutation and common mode voltage of the inverter.

A hybrid PWM strategy similar to (dos Santos et al., 2010b) for a two-level Z-source inverter is implemented for the Z-source NPC topology (Muniz et al., 2011) to reduce its algorithm calculation by combining the theory of SVPWM and triangular comparison PWM. A reduced component count Z-source NPC converter with modified modulation technique is reported in (Poh Chiang et al., 2009; Gao et al., 2007) using a single Z-source network. This topology reduces the requirement of an additional impedance network to create a neutral point as explained in (Poh Chiang et al., 2007b; Muniz et al., 2011). The modulation scheme is modified to create a full DC-link (FDCL) and a partial DC-link (PDCL) shoot-through state to boost the output voltage without increasing the commutation time as in the conventional NPC modulation techniques (Poh Chiang et al., 2007b). An effective control method for a cascaded quasi Z-source inverter using multilevel space vector modulation (MSVM) is presented in (Galigekere and Kazimierczuk, 2011) for single phase and in (Liu et al., 2013b) for three-phase to generate seven-level voltage.

This control scheme achieves independent control of Maximum Power Point Tracking (MPPT) for each photovoltaic panel and also balances the DC-link voltage across each H-bridge inverter to accomplish premium power quality for grid integration of photovoltaic panels for low switching frequency design. A summary of comparison of various modulation techniques for three-phase multilevel topologies is given in Table (3.6).

Table 3.6: Comparisons of various modulation techniques for three-phase multilevel topologies

Ref. No	Modulation technique	Topology	No. Of Switching	Device Stress	features
(Poh Chiang et al., 2007a)	Continuous	NPC with two Z-source networks	8(in EI)6 (in MR)	Medium	Symmetrical/Balanced voltage boosting per switching cycle. Small current ripple.
	Discontinuous	NPC with two Z-source networks	4	high	Balanced voltage boosting only per 60^0 cycles. Large current ripple and inductor size low common mode voltage. Low common mode voltage.
(Poh Chiang et al., 2007b)	NTV	NPC with two Z-source networks	6	medium	Completely eliminates the common-mode voltage
	RCM	NPC with two Z-source networks	6	Medium	Reduces common mode voltage.
(Poh Chiang et al., 2009)	FDCL	NPC with single Z-source network	4	Medium	Suitable for high switching frequency (due to minimum Commutation). Not particularly suitable for low-frequency operation. Fewer components. Low cost design.
	PDCL	NPC with single Z-source network	4	Medium	Suitable for high switching frequency (due to minimum Commutation). Not particularly suitable for low-frequency operation Fewer components. Low cost design. Comparatively better output waveforms.

(Yushan et al., 2014b, Jianfeng et al., 2011, Liu et al., 2013b)	MSVM	Single-phase qZSI-cascaded multilevel Inverter(CMI)	6	low	Independent control of MPPT for each module separately. Higher input-voltage utilization. Flexible to n-level (CMI).

3.3.4 Modulation Techniques for Matrix Converter Topologies

The matrix converter is a direct AC-AC converter with sinusoidal input/output waveforms and a controllable input power factor. Based on the conventional matrix switching topologies (Kolar et al., 2002), various impedance-network based direct (Baoming et al., 2012; Qin et al., 2012) and indirect (Karaman et al., 2014) matrix converter topologies are adopted in the literature for overcoming issues like improved reliability and higher voltage boost. With some modifications made to the conventional modulation techniques (SVPWM, carrier-based PWM, PWAM, etc.) to incorporate the shoot-through state, various modified modulation techniques are implemented to control direct and indirect impedance-network based matrix converters.

The traditional carrier-based sinusoidal PWM (SPWM) (Yan et al., 2013) is applied to control and modulate various Z-source and quasi-Z-source direct matrix converters with a few modifications, e.g., four control strategies: simple maximum-boost control, maximum-boost control, maximum-gain control and hybrid minimum-stress control are proposed in (Baoming et al., 2012). In the simple maximum-boost control, the modulation index is limited to M= 0.5 which means that the maximum voltage gain can only go up to 0.944. Maximum boost control utilizes all the zero states as shoot-through states.

The range of modulation index is extended to 0.866 by injecting 1/6 of the third harmonic signal in the reference signal. The maximum-gain control method can obtain the maximum gain at the same modulation index among all four techniques, and the hybrid minimum-voltage stress control can obtain the minimum voltage stress at the same voltage gain. In terms of the total harmonic distortion (THD) at the output, the maximum-constant-boost control method is effective in eliminating low-order harmonics compared to the simple boost and maximum boost controls. A comparison of various control methods is also presented in (Qin et al., 2011a).

A summary of different SPWMs is shown in Table (3.7). Pulse-Width-Amplitude-Modulation (PWAM) with a maximum-constant-boost shoot-through control strategy is also implemented in (Qin et al., 2012)to control a voltage-fed quasi-Z-source direct-matrix converter. This modulation technique reduces the switching frequency of the matrix converter by 1/3 compared to the SVPWM, which helps to reduce the switching losses by more than 50% compared to the SVPWM and 87% compared to the SPWM.

Table 3.7 comparisons of various modulation techniques for Z-source matrix topologies

Simple maximum-Boost Control	Maximum-Boost-Control	Maximum-Gain Control
$D_{st}=1-2\pi M/(3\sqrt{3})$	$D_{st}=1-M$	$D_{st}=0.5$ for $M\leq 0.5$
$B=[1-\frac{2\pi M}{3\sqrt{3}}+4\pi^2M^2/9]^{-1/2}$	$B=[3M^2-3M+]^{-1/2}$	$D_{st}=1-M$ for $M>0.5$
$G=[(\frac{1}{M}-\pi/\sqrt{3})^2+\pi^2/9]^{-1/2}$	$G=[(\frac{1}{M}-\pi/\sqrt{3})^2+\pi^2/9]^{-1/2}$	$G=2M$ for $M\leq 0.5$
$M\leq 0.5$	$M\leq 0.5$	$G=M[3M^2-3M+]^{-1/2}$ for $M>0.5$

3.3.5 Modulation Techniques for DC-DC converter with intermediate H-bridge

Various DC-DC converters are proposed in the literature using single-switch, two-switch and four-switch topologies. PWM for single-switch (Siwakoti et al., 2014b) and two-switch (Fan et al., 2008; Dong and Peng, 2009) topologies are fairly simple and can be achieved by controlling the duty cycle of the switch depending on the DC-link voltage. However, a DC-DC converter using an intermediate H-bridge as shown in Figure (3.16) involves more complex control, as four switches are required to be switched optimally to get the required output and performance.

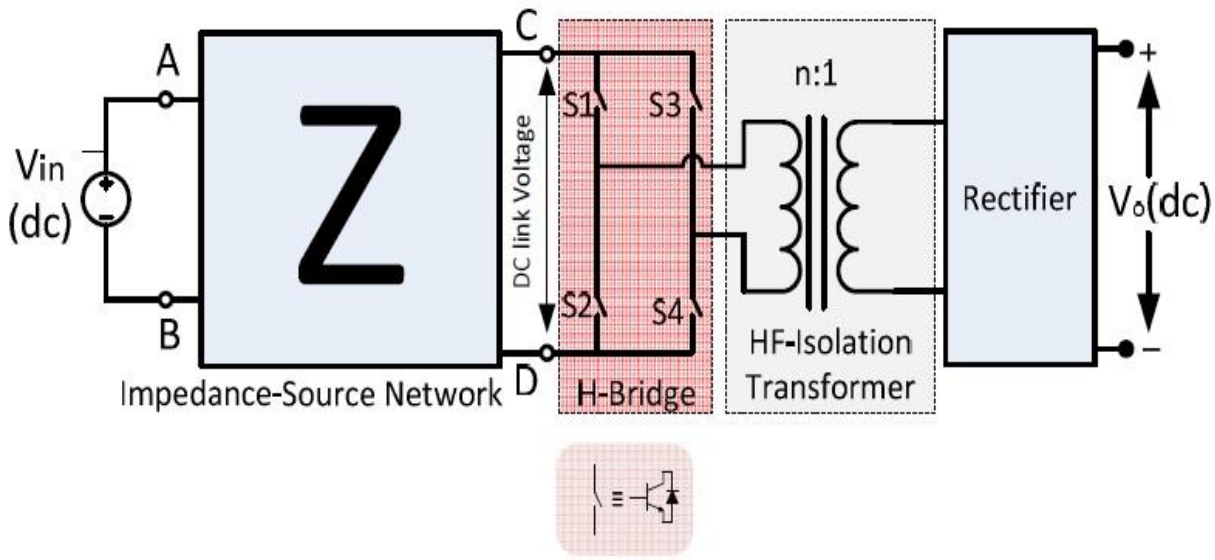


Figure 3.16 General circuit configuration of impedance-source network for DC-DC power conversion with intermediate H-bridge topology using various impedance-source networks.

Various modulation techniques are proposed in the literature, including shoot-through during freewheeling states, shoot-through during zero states, Phase Shift Modulation (PSM) control with shoot-through during zero states (Vinnikov and Roasto, 2011;

Nguyen et al., 2013), shoot-through by overlap of the active states (Hyeongmin et al., 2012) and shifted shoot-through (Roasto et al., 2013). Due to shoot-through insertion in PWM, the switches in the H-bridge are compelled to commute at 2-3 times higher than the switching frequency. In shoot-through during freewheeling states, the top-side and bottom-side switches of the inverter bridge operate at three times the switching frequency $f_{sw,top} = 3f_s$ and $f_{sw,bottom} = 3f_s$ as shown in Figure (3.17).

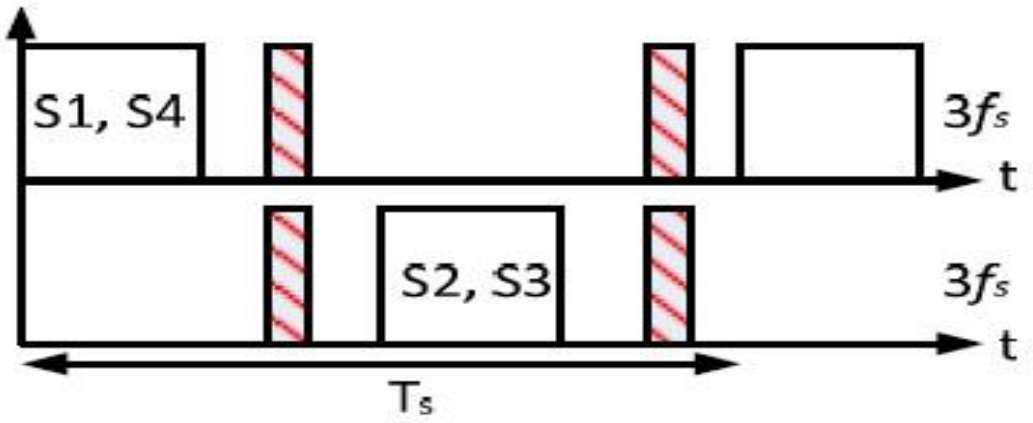


Figure 3.17 shoot-through during freewheeling states

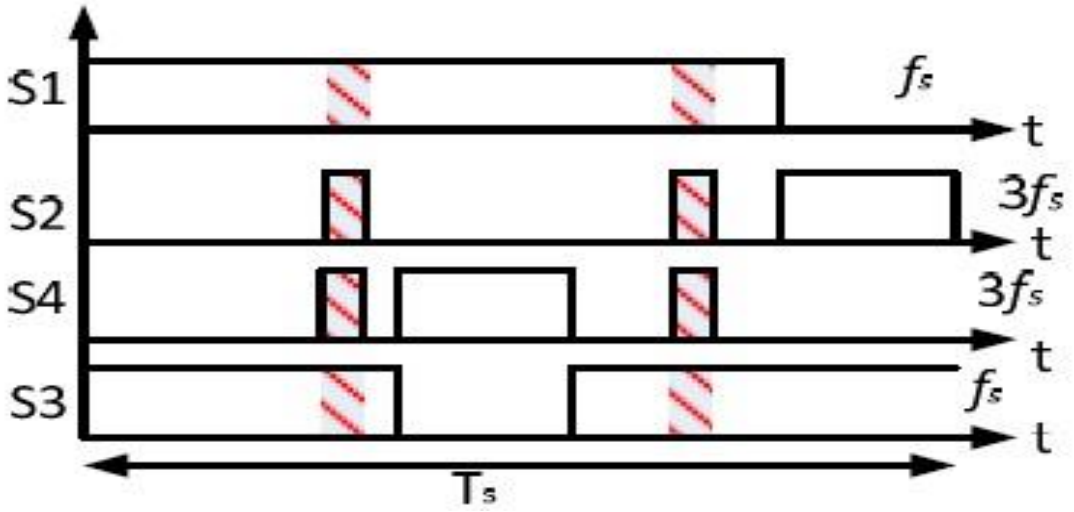


Figure 3.18 shoot-through during zero states

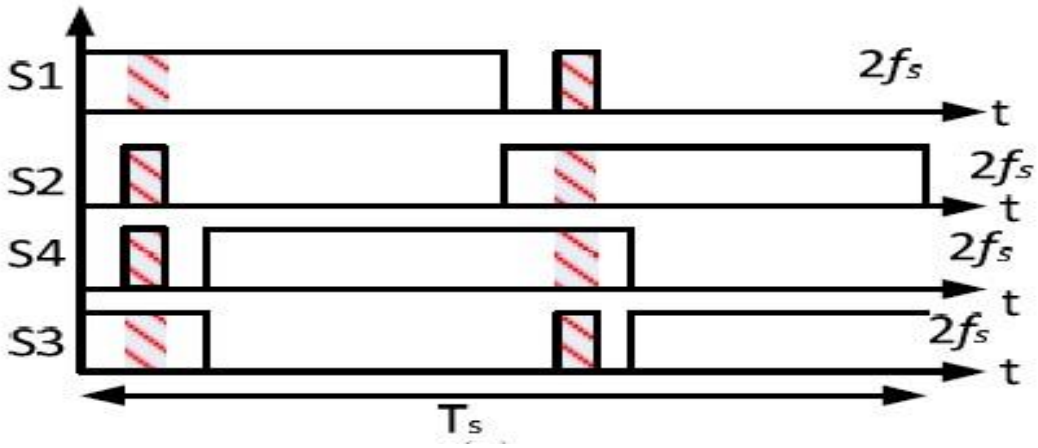


Figure 3.19 phase-shift modulation (PSM) control with shoot-through during zero states

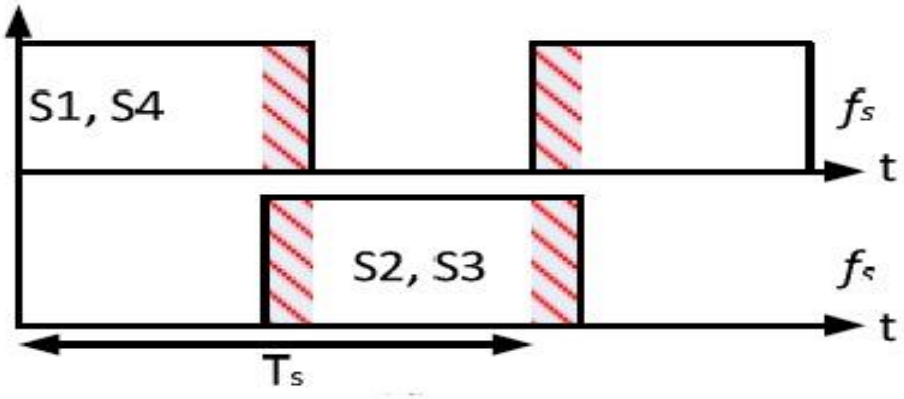


Figure 3.20 shoot-through by the overlap of active states

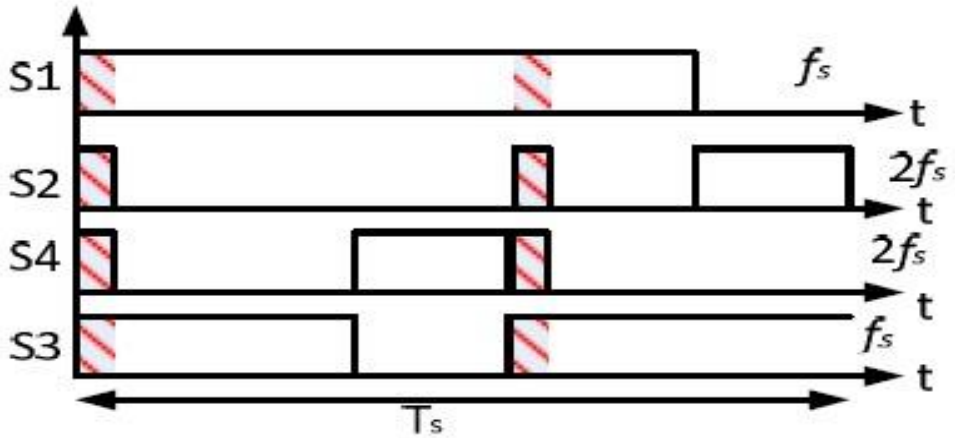


Figure 3.21 Shifted shoot-through (→Shoot-through)

This leads to a high switching loss. Similarly, the number of commutations of the bottom-side switches remains the same while reducing the switching frequency of the topside switch $f_{sw,top} = f_s$ and $f_{sw,bottom} = 3f_s$in the shoot-through during zero states modulation techniques (see Figure (3.18)). Phase Shift Modulation (PSM) control with shoot-through during zero states (see Figure (3.19)) equalizes the switching losses of the top-side and bottom-side switches ($f_{sw,top} = 2f_s$ and $f_{sw,bottom} = 2f_s$), but this method is not effective in reducing the commutation time of the switches. The switching loss is minimized in shoot-through by the overlap of active states ($f_{sw,top} = f_s$ and $f_{sw,bottom} = f_s$as shown in Figure (3.20); however, the active-state and shoot-through state duty cycles are not independently controllable. The inter-dependency of the active-state and shoot-through state duty cycle could cause problems in the output-voltage compensation and also for systems which require independent control of active and shoot-through state.

A shifted shoot-through modulation technique (see Figure (3.21)) could reduce the switching frequency of the switches, but it is complex and difficult to implement particularly in the microcontroller due to large number of comparator requirement. It also requires additional external components (logic gates, etc.) for implementation. The major disadvantage of this modulation technique is the loss of full soft-switching properties. Every addition of the shoot-through state increases the commutation time of the semiconductor switches and so increases the switching loss in the system. Hence, minimization of the commutation time by optimal placing of the shoot-through state in a switching time period is necessary in order to minimize the switching loss.

A detailed comparison of the different modulation techniques considering theoretical complexity and performance is shown in Table (3.8).

Table 3.8: Comparison of modulation techniques for dc–dc converter with an intermediate h-bridge

Parameters	Method A	Method B	Method C	Method D	Method E	Method F
Maximum switching frequency of top-side transistors	$3f_s$	f_s	$2f_s$	f_s	f_s	f_s
Maximum switching frequency of bottom-side transistors	$3f_s$	$3f_s$	$2f_s$	f_s	$2f_s$	$2f_s$
Independent active and shoot-through state controllability (for voltage compensation)	Yes	Yes	Yes	No	Yes	yes
Measured maximum transient overvoltage on top-side transistors	1.5pu	2.4pu	2.5pu	2.1pu	1.6pu	1.3pu
Measured maximum transient overvoltage on bottom-side transistors	2.6pu	1.85pu	2.5pu	2.1pu	>2pu	1.3pu
Measured maximum transient overvoltage on capacitor C1	1.7pu	1.7pu	1.2pu	1.7pu	-	1.2pu
Measured maximum transient overvoltage on capacitor C2	1.5pu	1.5pu	3.5pu	1.5pu	-	1.2pu
Soft-switching for top-side transistors	Partial	Full	-	No	Partial	Full
Soft-switching for bottom-side transistors	Partial	No	-	No	Partial	partial
Complexity of implementation (1 to 6 in increasing order of complexity)	3	4	5	2	6*	1

*difficult to implement in microcontroller and requires some additional hardware.

Method A: Shoot-through during freewheeling states.

Method B: Shoot-through during zero states.

Method C: Phase-Shift Modulation (PSM) control with shoot-through during zero states.

Method D: Shoot-through by overlap of active states.

Method E: Shifted Shoot-through.

Method F: Optimized PWM control with shoot-through during zero-states.

3.4 Losses, Harmonics and EMI

For designing the electric power system, three major issues come to matter, such as Losses, Harmonic and Electromagnetic Interference (EMI). The mentioned issues affect the system in terms of quality, efficiency, size and cost. Therefore, there is a trade-off between these factors. The key factor in power converter is power switches; they have been categorised based on capability on handling of the power and their switching speed to maximise the voltage blocking and carrying current.

Achieving high efficiency, this is a key factor in the modern-day power convertors and defined for saving energy and reducing losses. It is a challenging task to achieve a desirable efficiency in convertors; for obtaining a great efficiency compromising between power density and quality is necessary.

Reducing the total loss is achievable by reducing the switching frequency and increasing the time of the switching which lead to increasing the EMI and decreasing the converter quality as the output current/voltage ripple is increasing.

3.4.1 THD and effects in Power Electronic Systems

The power regulation and consumptions are getting effected by distribution system's power quality. John Lundquist from university Chalmers, states "the phrase 'POWER QUALITY' has been widely used during the last decade and includes all aspects of events in the system that deviates from normal operations." The distortion appeared in power system, caused by new electric power sources in 20th century proved John's statement.

The harmonic distortion on the waveform is from power source as a nonlinear load. These harmonics can cause problems; ranging from telephone transmission interference to degradation of conductors and insulating material in motor and transformers. Therefore, measuring the total impact of these harmonics on the system is necessary. The summation of all harmonics in the system is known as Total Harmonic Distortion (THD). This section will discuss on THD's concept and its effects on electric systems.

3.4.2 Total Harmonic Distortion

Complexity of THD makes the concept very confusing and tough to grasp. Nevertheless, the concept will become easier to understand if broken down into different parts, such as the basic definitions of harmonics and distortion. Fig (3.22) shows an electric power system with an electrical load and ac-source.

According to the type of the loads (Non-linear, Linear), the quality of the power will get affected. This is due to the current drawn by the mentioned type of loads.

- In such non-linear devices, the current is not proportional to applied voltage.
- Mostly, odd harmonics are present in the system.
- Majority of nonlinearities in the system can be found in shunt elements loads.

Figure 3.22 Power System with AC source and electrical load

Linear loads in general do not distort the waveforms; they draw current which is sinusoidal in nature as can be seen in Figure (3.23). Linear loads mostly used in households appliances. On the other hand, none-linear loads draw current wave which is not perfectly sinusoidal as can be seen in Figure (3.24). Voltage wave-distortion are generated, since the current-wave deviated from sin-wave.

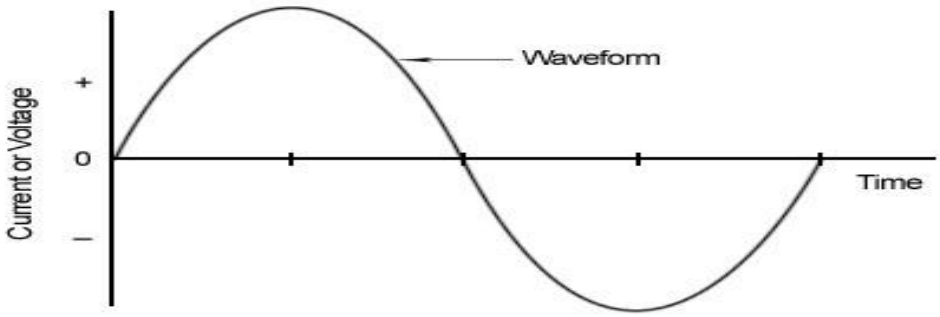


Figure 3.23 Ideal sine wave

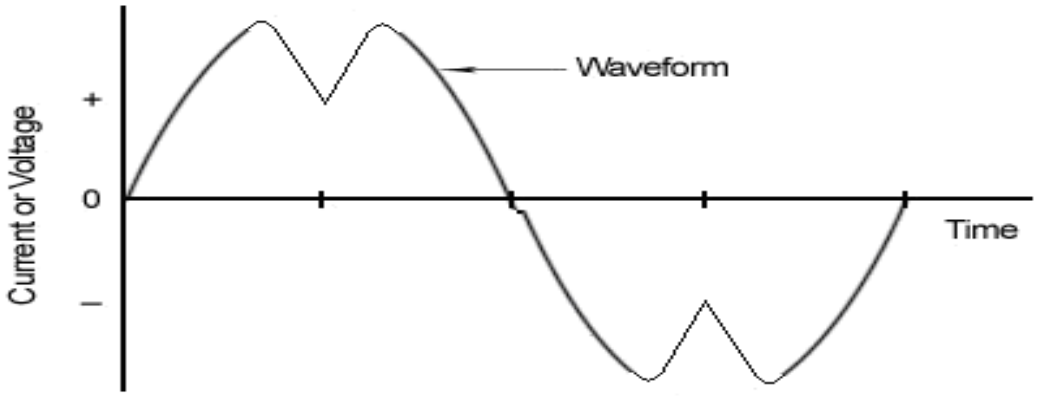


Figure 3.24 Distorted waveform

The shape of the sinusoidal wave is changing drastically as can be seen in Figure (3.24). However, no matter the level of complexity of the fundamental wave, it is actually just a composite of multiple waveforms called harmonics. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For instance for the fundamental waveforms of 50Hz, the second, third, fourth and fifth harmonic component would be 100 Hz, 150 Hz, 200Hz and 250Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The harmonic component in ideal sinusoidal waveform is equal to zero, which means for the pure sine-wave there is nothing to distort the waveform. As mentioned earlier, the fundamental components of current/voltage waveform are compared against summation of all harmonic elements of current or voltage waveform:

$$THD_{Voltage} = \frac{\sqrt{V2^2+V3^2+V4^2+\cdots+Vn^2}}{V1} * 100\% \qquad (3.1)$$

$$THD_{Current} = \frac{\sqrt{I2^2+I3^2+I4^2+\cdots+In^2}}{I1} * 100\% \qquad (3.2)$$

The equations above indicate the THD on a voltage and current signals. Results has been calculated in percentage which is the comparison of fundamental component of the signals with harmonic component. The greater the result is, will proof that there is more distortion is presented on the main signals.

3.4.3 Voltage vs. Current Distortion

- The source of the shunt's current harmonics along with injected current harmonic to the system appears to be the nonlinear loads.
- The outcome of passing distorted currents through the linear will be in voltage distortion, series impedance of the power delivery system.
- Harmonic currents passing through the impedance cause a voltage drop for each harmonic. This results in voltage harmonic appearing at the load bus.
- Voltage distortion is the outcome of load current harmonic and the load has no control over voltage distortion.
- Current harmonic control is at the end-user applications.
- Control over the voltage distortion, assuming the harmonic current injection is within reasonable limit, is exercised by the entity having control over the system impedance, which is often the utility.

3.4.4 The Usual Suspects

Existence of harmonic on electrical system is from the first generator. Nonetheless, neglecting the small harmonic components before 1960s due to lack of nonlinear loads. As in university of Wollongong associated professor, V.J. Gosbell stated,

“Harmonic distortion is not generally due to the operation of the power system, and was largely absent before the 1960s. At about this time, a different type of customer load with electronic power supplies became popular.” This was the beginning of the era of non-linear loads which now include electronic ballasts, computer power supplies, fax machines, arc furnaces and variable frequency drives (VFDs). Harmonic distortion can have detrimental effects on electrical equipment. Unwanted distortion can increase the current in power systems which results in higher temperatures in neutral conductors and distribution transformers. Higher frequency harmonics cause additional core loss in motors which results in excessive heating of the motor core. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperatures and interference can greatly shorten the life of electronic equipment and cause damage to power systems.

3.4.5 Importance of Mitigating THD

There is no limitation has been set up on the system for THD, but there are some recommendation regarding acceptable harmonic distortion. IEEE Std 519, “RECOMMENDED PRACTICES AND REQUIREMENTS FOR HARMONIC CONTROL IN ELECTRICAL POWER SYSTEMS” provides suggested harmonic values for power systems:

“Computers and allied equipment, such as programmable controllers, frequently require AC sources that have no more than 5% harmonic voltage distortion factor

(THD), with the largest single harmonic being no more than 3% of the fundamental voltage. Higher levels of harmonics result in erratic, sometimes subtle, malfunctions of the equipment that can, in some cases, have serious consequences." (IEEE Std 519, 2014).

Hence the limitation of THD for voltage harmonic is at 5% and single harmonic is at 3%. It should be noted the given standard limits are voluntary. Nevertheless, to increase the life span and performance of the system, the THD value has to be kept as low as possible.

3.5 Summary

This chapter has presented an exhaustive review of modelling, control and modulation techniques for impedance source networks for power converters. A broad classification of the modulation techniques into five categories with further sub-classification aims to provide easy selection of control and modulation techniques for appropriate topologies for particular application. Further, a comparison of various modulation techniques for particular switching topologies based on theoretical complexity and performance informs the selection of the correct control and modulation technique for the respective switching topologies to achieve maximal voltage boost, minimal harmonic distortion, lower semiconductor stress and a minimal number of device commutations per switching cycle.

Chapter 4

Circuit design and Analysis

4.1 High Performance Bidirectional Quasi-Z-Source inverter design and analysis

Modified high performance bidirectional quasi-Z-source overcomes the limitations of conventional QZSIs. This new design simplifies the controller design and has an advantage of operating in wide-range of load even no load with the smaller inductors which eliminates the probability of voltage drop in DC-link. Operating models, analysis, voltage relations for the new high performance bidirectional quasi-Z-source inverter along with control technique for extra switch is brightly explained.

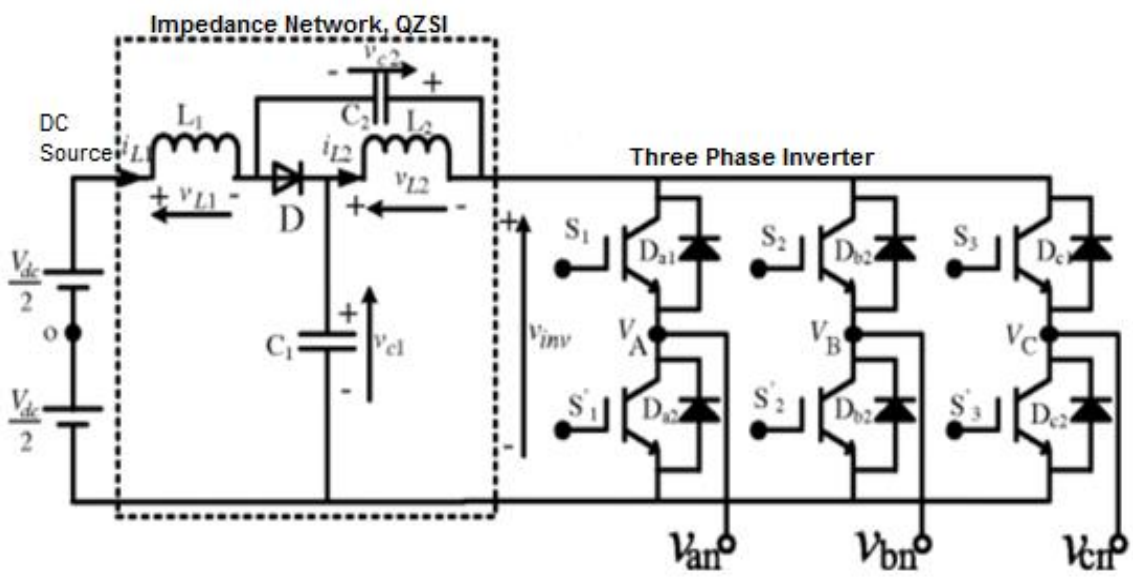


Figure 4.1 Traditional impedance network quasi-z-source inverter

In order to design the high performance bidirectional quasi-Z-source network and analyse the power loss, the voltage and current of the capacitor, inductors, and switching devices needs to be derived. As mentioned previously QZSIs are very well-matched for renewable energy power conditioning systems. Figure (4.1) shows the traditional impedance network quasi-z-source inverter.

Full bridge inverter cell can produce three possible output voltages such as $+Vs$, 0 and $-Vs'$. In comparison to the conventional inverters, new design has an extra switching states called shoot-through state which occurs in null state that the DC-link is short circuited and its voltage is zero. Depend on pulse width modulation method used in the system, replacing all null state by shoot-through state in boost mode is achievable. In new switching state, capacitors are charging the inductors whereas in active state the inductors and input DC source is discharging by the load. Hence voltage gain is improved.

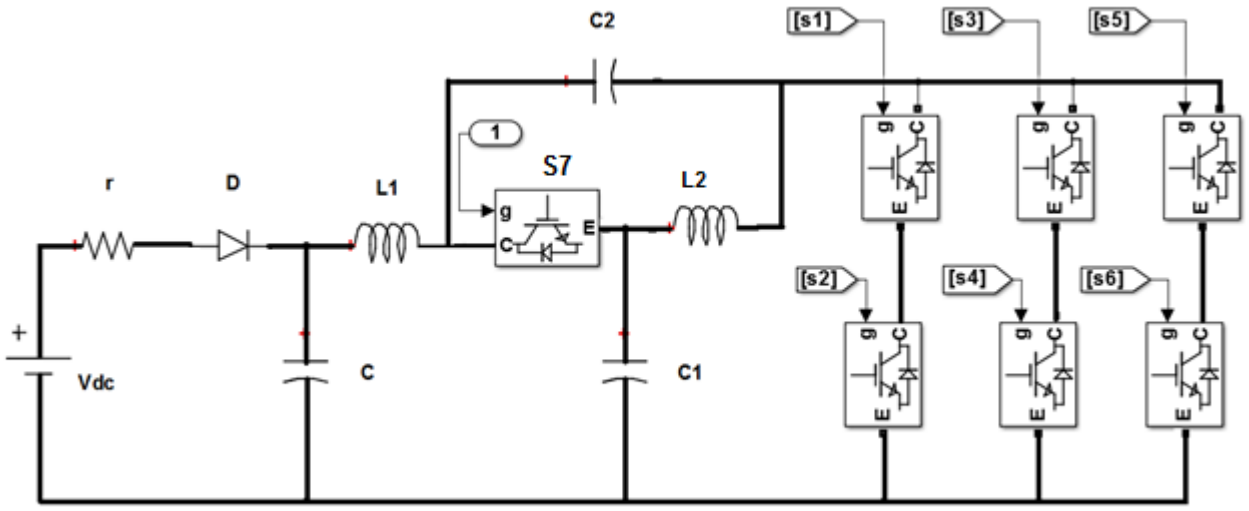


Figure 4.2 New high performance Bidirectional quasi-Z- source network

4.2 Operation modes and characteristics of High Performance Bidirectional QZSI

The literature illustrates numerous topologies of QZSIs. This part describes the voltage-fed HPB-QZSI with continuous input current, as shown in Figure (4.1) The conventional Bidirectional QZSI has two general operating states which are the active state and the shoot-through state (Ellabban and Abu-Rub, 2012; Ellabban et al., 2013). In shoot-through state time period, the upper switch and lower switch in the same leg of the three-phase bridge conducting at the same time to increase the DC-link voltage. Figure (4.2) shows the HPB-QZSI topologies consist of two parts as follow:

First part includes of C, C1, C2, L1, L2, and switch7 (S7) and second part is the three-phase bridge. In comparison with the conventional QZSI the diodes in the network substituted by S7 with a parallel body diode which with an appropriate controlling of S7 the bi-directional power flow can be realised. During the regeneration mode, the switching pattern of S7 is complementary with the shoot-through pattern of the three phase bridge. When the three-phase bridge is in the shoot-through state, S7 is open. The body diode is reversely blocked and the voltage boost function can be realised. When the three-phase bridge is in the non-shoot-through state, S7 is closed. The seven operational modes of shoot-through zero state and non-shoot through along with equivalent circuit in operating modes period are shown as follow:

4.2.1 Mode 1

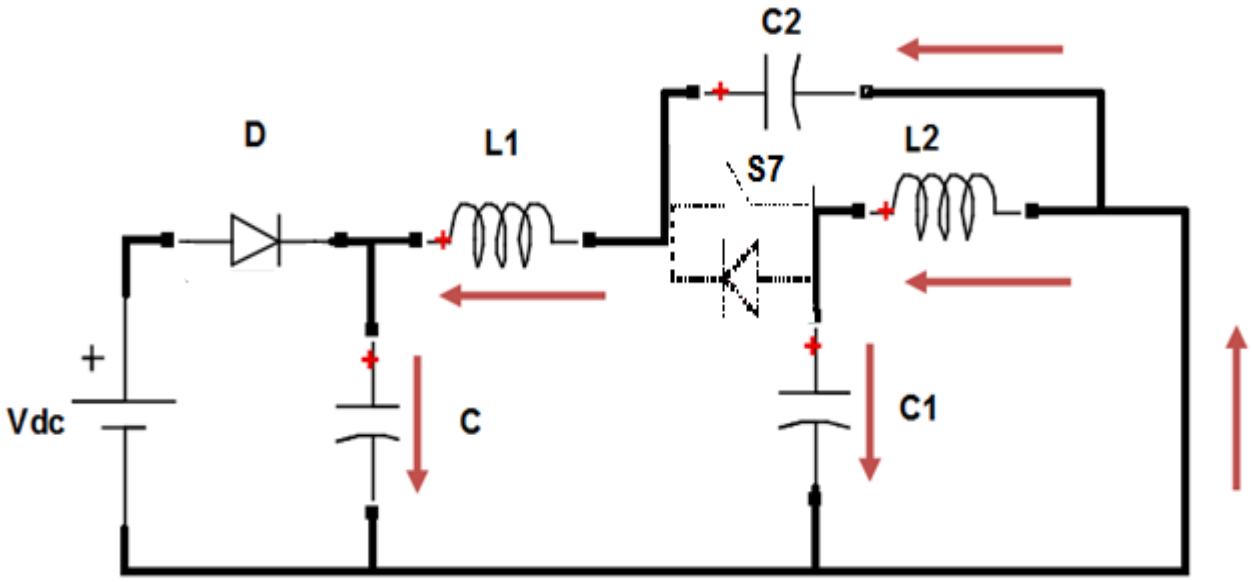


Figure 4.3 Mode 1a

In shoot-through operation mode S7 is OFF since $Vc1 + Vc2 > Vin$; therefore, reverse current will be barred. Current in inductors will be discharged and capacitors will be charged up as shown in Figure (4.3).

For safety purposes of reversing current and enhancing the performance, diode D and capacitor C needs to be placed between the B-QZSI and DC source. Otherwise, the two capacitors in the QZSI network may be short-connected through S7, which will cause damage of the devices.

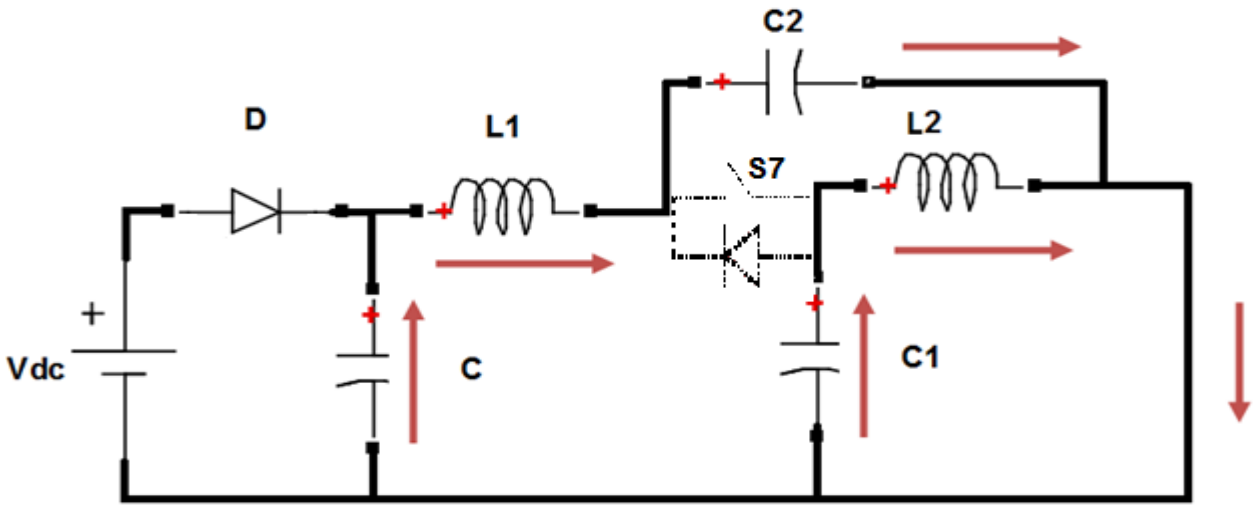


Figure 4.4 Mode 1b

As far as the shoot-through time period is long enough probability of changing direction of the inductor's current is high to discharge the capacitors and charge-up the inductors. [See Figure (4.4)]

4.2.2 Mode 2

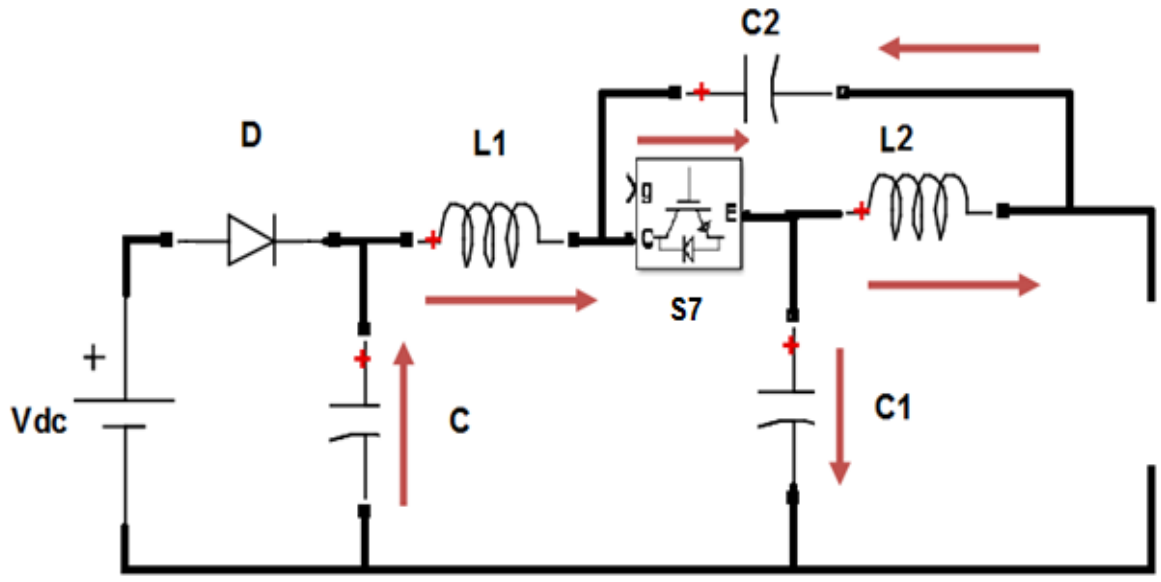


Figure 4.5 Mode 2

In the case of long shoot-through time period with the positive direction of current in inductors, the HPB-QZSI will go to Mode2, otherwise Mode7; that will be described later. In Mode2 the HPB-QZSI is operating in null state and switch7 is ON, which current flow through S7. The current in inductors is decreasing, whereas the voltage of the capacitors is charging up. This mode only exists when the inductance is small or the power factor is low. [See Figure (4.5)]

4.2.3 Mode 3

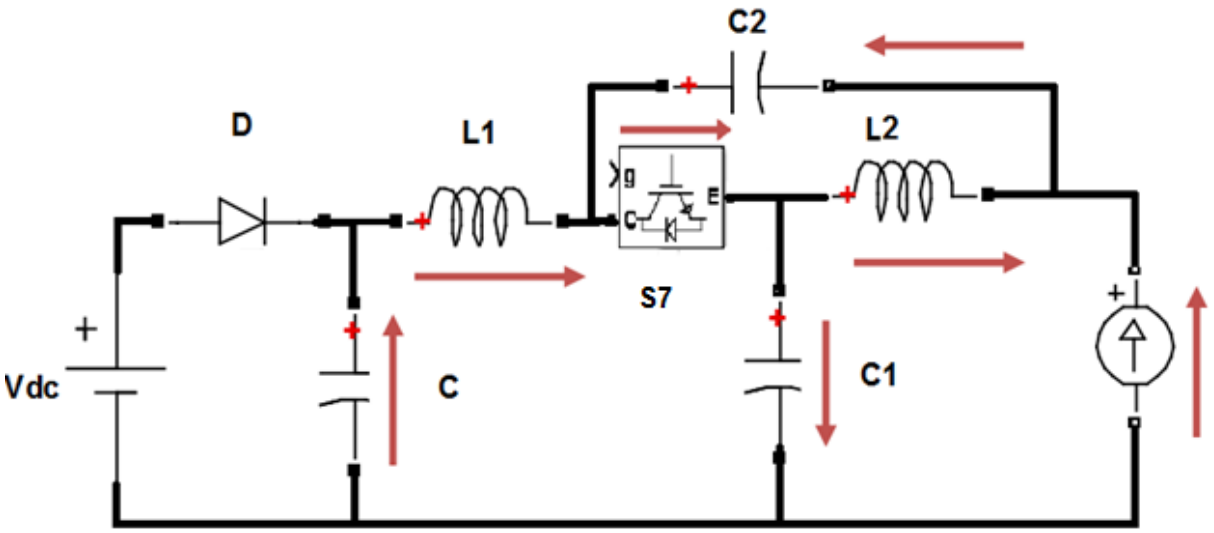


Figure 4.6 Mode 3

In Mode3, the HPB-QZSI is operating in active state and the direction of the currents in inductors is the same as Mode2 which the inductor's currents are continuously decreasing while charging up the voltages of the capacitors. This mode only exists when the inductance is small or the power factor is low. [See Figure (4.6)]

4.2.4 Mode 4

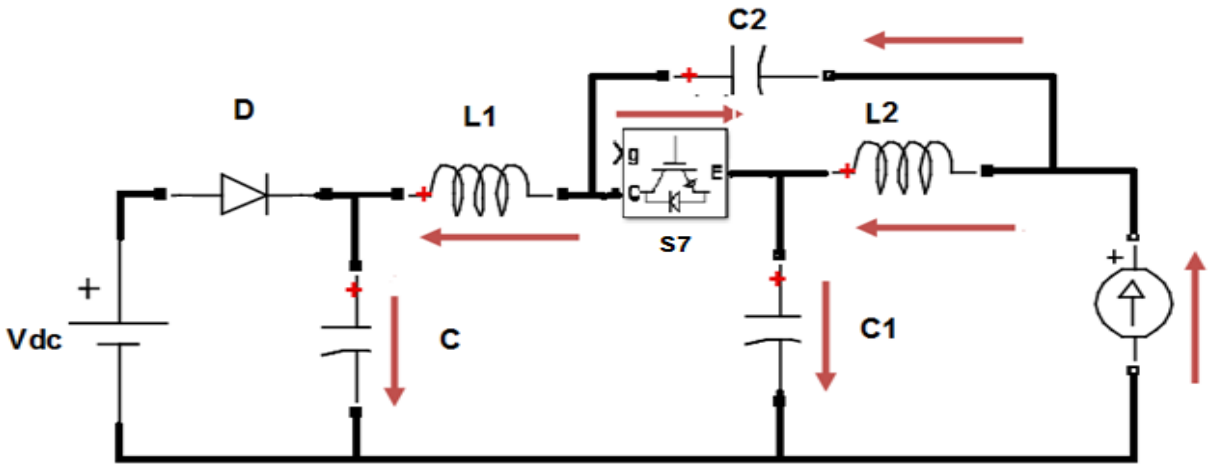


Figure 4.7 Mode 4

The HPB-QZSI operates in Mode3 until the inductor current reaches zero. Mode4, operates when I_L < 0, and $|I_L|$ < $|I_O|/2$. The current in inductors is decreasing, whereas the voltage of the capacitors is charging up with active-power. This mode only exists when the inductance is small or the power factor is low. [See Figure (4.7)]

4.2.5 Mode 5

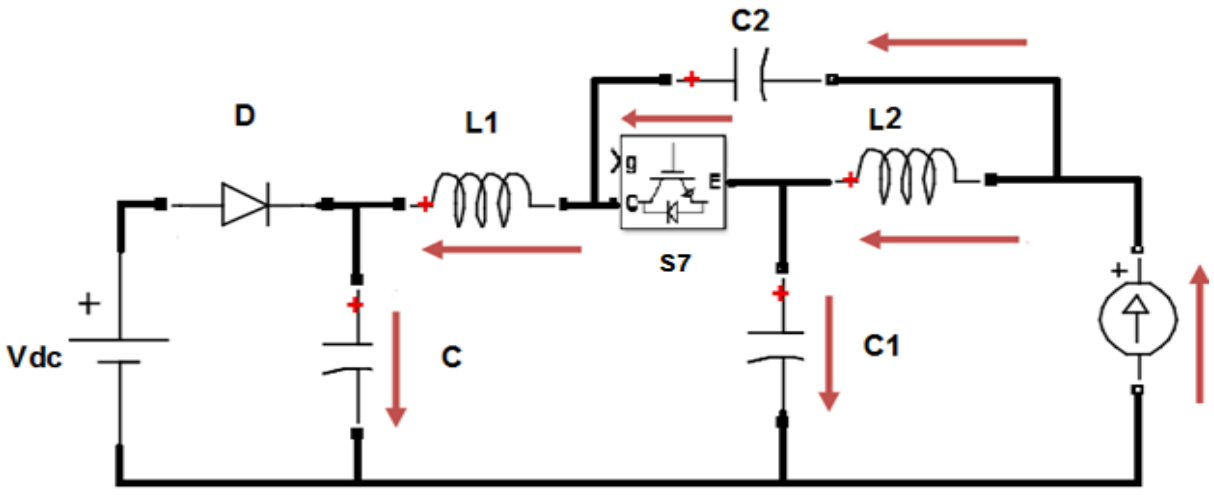


Figure 4.8 Mode 5

Operating in Mode5, when I_L < 0, and$|I_O|/2 < |I_L| < |I_O|$. The current in inductors is decreasing, whereas the voltage of the capacitors is charging up with active-power which is the same as Mode4, however the direction of current in Mode5 for S7 has changed. [See Figure (4.8)]

4.2.6 Mode 6

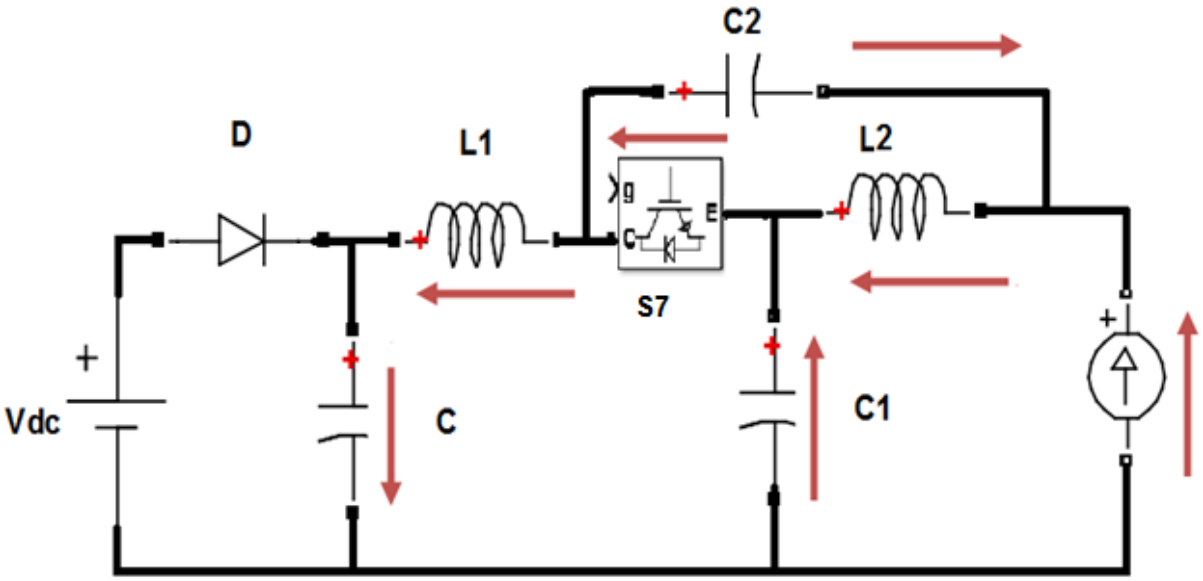


Figure 4.9 Mode 6

The HPB-QZSI is in Mode6 when I_L < 0 and $|I_L| > |I_O|$ in this mode, the capacitor voltages begin to drop, and the inductor currents continue to increase. [See Figure (4.9)]

4.2.7 Mode 7

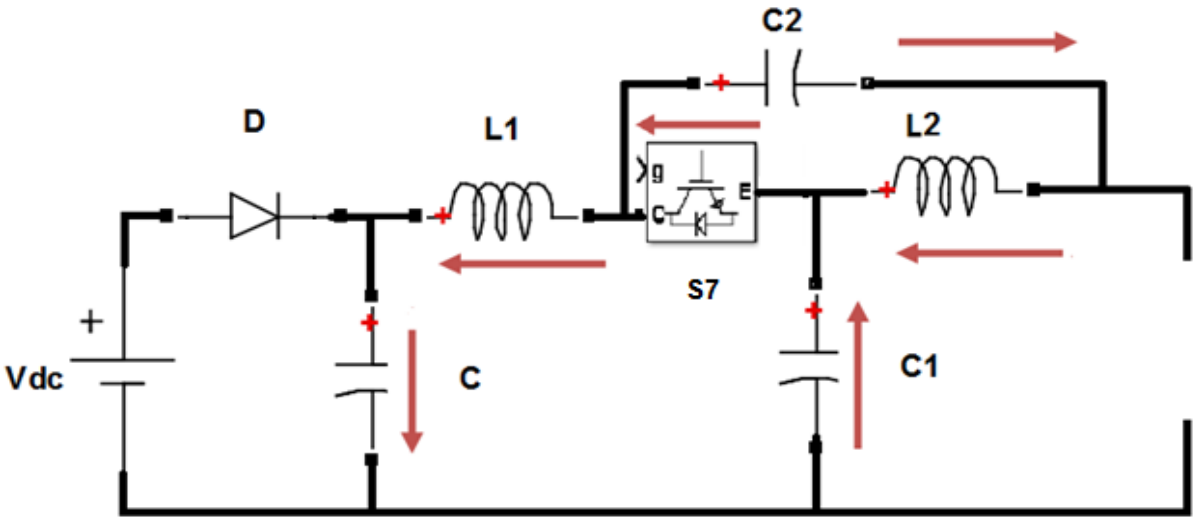


Figure 4.10 Mode 7

The HPB-QZSI is in the null state. In Mode7, the voltage of the capacitor is continuously discharging while the inductors are charging-up. In HPB-QZSI the inductor current is continuously flowing. If the same switching pattern of S7 is implemented in the motoring mode, unlike the traditional QZSI, the reverse current in the inductors will no longer be cut off by the diode. Instead, it can continuously flow through S7 in the reverse direction [See Figure (4.10)]. Therefore, the DCM of the QZSI can be avoided (Miaosen and Fang Zheng, 2008a) and the performance of the inverter will be improved. This is particularly helpful in electric motor drive application, where the power factor of the motor is low with a light load.

4.3 Voltage Relationships

4.3.1 Non-shoot Through

When the inverter operates in non-shoot through zone, continuous reduction of current in inductor makes S7 to be in ON-state conduction mode, therefore supplying the inverter from input DC voltage and capacitor C to charge up the $C1$ and $C2$ of the HPB-QZSI. According to the circuit from Figure (4.6), the voltage relationships in non-shoot through time (T_{nsh}) is as follow:

$$V_{L1} = V_C - V_{C1} \qquad V_{L2} = -V_{C2} \quad (4.1)$$

$$V_O = V_{C1} - V_{L2} = V_{C1} + V_{C2} \quad (4.2)$$

Where,V_{L1}, V_{L2}, V_{C1} and V_{C2} are inductor voltage and capacitor voltage respectively. V_O is the output voltage and V_C is the input capacitor voltage.

$$I_{C1} = I_{L1} - I_O \quad (4.3)$$

$$I_{C2} = I_{L2} - I_O \quad (4.4)$$

Where I_{C1}, I_{C2}, $I_{L1}$and I_{L2} are capacitors current and inductors current respectively. I_O, the output current.

4.3.2 Shoot-Through

The system operates in shoot-through time period as the sum of voltages of the network capacitors are more than input DC voltage ($V_{C1} + V_{C2} > V_{dc}$), therefore S7 is in OFF-state and inductors are charging up through C1 and C2. According to the circuit from Figure (4.3), the voltage relationships in shoot through time (T_{sh}) is as follow:

$$V_{L1} = \bar{\upsilon}_{L1} T_s = T_{sh}\,(V_{c2} + V_{dc}) + T_{nsh}\,(V_{dc} - V_{c1}) = 0 \quad (4.5)$$

$$V_{L2} = \bar{\upsilon}_{L2} T_s = T_{sh}\,(V_{c1}) + T_{nsh}\,(-V_{c2}) = 0 \qquad (4.6)$$

WhereT_s,T_{sh} and T_{nsh} are switching time, shoot-through time and non-shoot-through time respectively.

Thus the following relations are

$$V_{C1} = (1-D)/(1-2D)\; v_{dc} \qquad (4.7)$$

$$V_{C2} = \frac{D}{1-2D} v_{dc} \qquad (4.8)$$

From equations (4.2), (4.7), and (4.8) we can calculate the peak DC-Link voltage.

$$V_O = V_{c1} + V_{c2} = \frac{T_s}{T_{nsh}-T_{sh}} v_{dc} = \frac{1}{1-2D} v_{dc} = B v_{dc} \qquad (4.9)$$

Where, D is duty ratio and B is the boost factor for the HPB-QZSI. The average currents through the two inductors L_1 and L_2 can be calculated by the system power rating P:

$$I_{L1} = I_{L2} = I_{in} = P/v_{dc} \qquad (4.10)$$

According to Kirchhoff's current law and equation (4.8), the following current relations are obtained:

$$I_{c1} = I_{c2} = I_o - I_{L1} \qquad (4.11)$$

Where, I_{c1}, I_{c2}, I_{L1} are the capacitors current and inductors current respectively. I_O is the output current.

Boosting the system in HPB-QZSI is achievable with shoot-through insertion to the DC-link periodically. At the times of shoot-through the current in inductors are increasing and by the termination of shoot-through time period, the energy will transfer to the capacitor and load. The capacitor's voltages are rising and the inductor's currents are sinking again.

In steady-state, the average voltages across the inductors and the average currents through the capacitors are zero, which leads to the following steady-state relations:

$$\bar{\upsilon}_{DC} = VI + \bar{\upsilon}_{C1} = \bar{\upsilon}_{C2} \qquad (4.12)$$

$$\bar{\mathrm{I}}_{L1} = \bar{\mathrm{I}}_{L2} = \bar{\mathrm{I}}_{DC} \qquad (4.13)$$

The output voltage stress decrease as modulation index increases; therefore with the specific voltage gain (G) in HBP-QZSI can keep the modulation index high, which decrease the voltage stress to the minimum. The design of inductor in HPB-QZSI is to eliminate the ripple of high frequency to $ri\%$ of highest inductor current in shoot-through time period.

In shoot-through time period the voltages of $L1$ and $L2$ are equal to $(V_{IN} * D_{nsh})/\ (D_{nsh} - D_{sh})$. Hence $L1$and $L2$ can be calculated by:

$$L_1 = V_{in} \frac{D_1 T_{sh}}{(D_{nsh} - D_{sh}) ri\ \%\ I_{L_1 max}} \qquad (4.14)$$

$$L_2 = V_{in} \frac{D_1 T_{sh}}{(D_{nsh} - D_{sh}) ri\ \%\ I_{L_2 max}} \qquad (4.15)$$

Where, $I_{L_{1max}}$ and $I_{L_{2max}}$ are the maximum value of I_{L1} and I_{L2}, respectively.

The design of $C2$ is to eliminate the ripple of high frequency to $rv\%$ of highest capacitor voltage V_{C2} which the current through C2 in shoot through time is equivalent to the I_{L1}. $C2$ can be calculated by:

$$C_2 = I_{L1} \frac{T_{sh}}{rv\%\ V_{C2max}} \qquad (4.16)$$

4.4 Performance Analysis of the Modulation Schemes

The main purpose of modulation method is to achieve and improve the voltage gain and decrease the total-harmonic-distortion (THD) as much as possible. There is a difference between HPB-QZS inverter and H-Bridge-Inverter; the method of inserting shoot-through time period is influencing the design and efficiency of the inverter. One of the unique characteristics of HPB-QZSI is the variation of AC-voltage between 0 to ∞ without considering the input DC-voltage.

A controllable shoot-through modulation techniques for voltage-fed HPB-QZS DC-AC inverter is described. Unique feature of new control strategy is reducing commutation time and decreasing losses in the switches. Active state period and shoot-through zero state can be controlled separately which allows the shoot-through time period get to the maximum limit $D_{st,max} = 0.5$. Hence, achieving a desire voltage gain for the application that sources is renewable energy such as photovoltaic, fuel cell, etc.

The ratio of the amplitude of the carrier signal and the control signal is called ‘amplitude modulation ratio’ or ‘modulation index’:

$$m = |V_m|/|V_C| = V_m/V_C \qquad (4.17)$$

When the modulating signal is less than equal to the carrier signal, it is called the ‘linear modulation region.’ When the amplitude of the modulating signal becomes more than the carrier signal, it is called the ‘pulse dropping mode’ or the ‘over modulation region’. The name is given because some of the edges of the modulating signal will

not intersect with the carrier. The modulating signal is then modified accordingly. Another parameter defined by the SPWM is called the 'frequency modulation ratio', and is given as:

$$m_f = f_c/f_m \qquad (4.18)$$

Where f_c is the frequency of the carrier and f_m is the modulation frequency. This is also an important parameter that decides the harmonic performance of the output voltage. The inverter leg switching frequency is equal to the frequency of the carrier signal and the switching period is:

$$T_C = 1/f_C \qquad (4.19)$$

$D_{ST} = T_0/T$, is the shoot-through time period, increasing the voltage of output is because of inserting shoot-through into switching states. The main aim of this strategy is to control the shoot-through insertion as the inverter is short circuited and the voltage of the output is zero. To have a sine-wave in the output some or all null state has to be replaced by shoot-though.

4.4.1 Three-phase PWM Voltage Source Inverter

Voltage-type-source inverters are considered here because voltage-type-inverters are generally more established and can conveniently be constructed using low-cost, high-performance insulated gate bipolar transistor (IGBT) modules (with integrated anti-parallel diode) or intelligent power modules. With the same topology as that of a conventional VSI, a voltage-type-source inverter can assume all active

(finite output voltage) and null (0 V output voltage) switching states of VSI. But unlike the conventional VSI where dead-time delays are inserted to the complementary switching of the two switches of a phase-leg to prevent short-circuiting of the phase leg. A voltage-type-source inverter has the unique feature of allowing both power switches of a phase-leg to be turned ON simultaneously (shoot-through state) without damaging the inverter.

Figure (4.11) shows three-phase voltage-fed electric power conversion system.V_A, V_B ,V_C are the voltages of the pole/leg which during the top switches operation can attain the value of +0.5 V_{DC} and in the period of bottom switches operation can get to $-0.5\ V_{DC}$ .The phase voltage applied to the load is denoted by the letters v_{an}, v_{bn}, v_{cn}. The operation of the upper and the lower switches are complimentary.

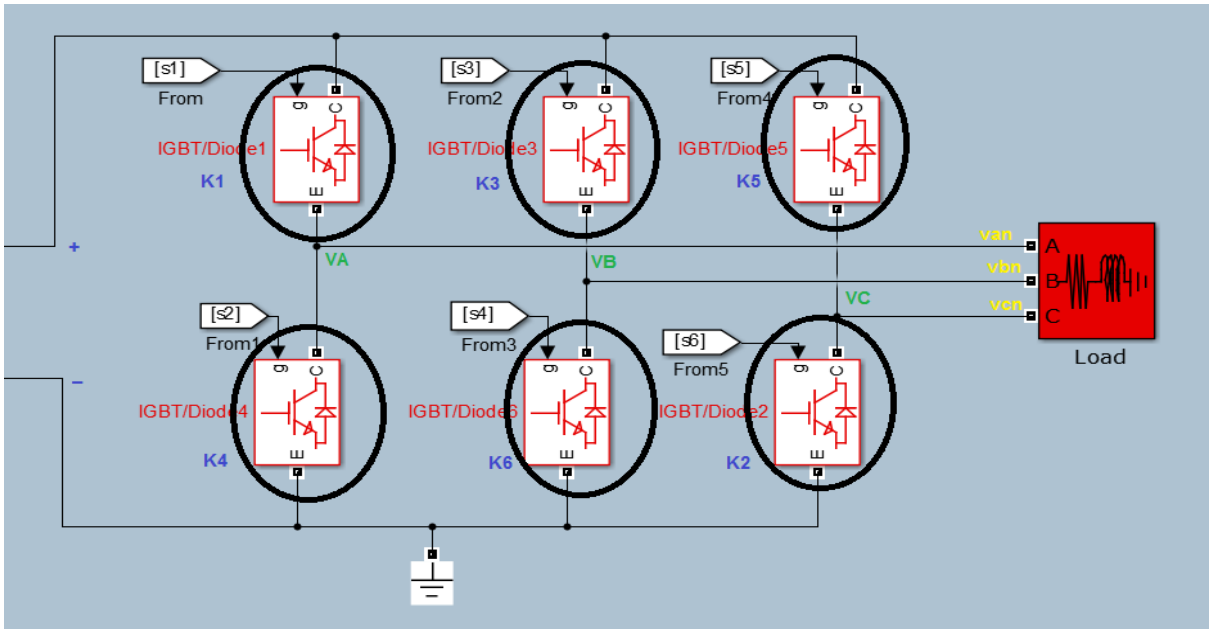


Figure 4.11 inverter switching

The relation between switching signal and leg voltage is as follow:

$$V_k = S_k V_{DC};\ K \in A, B, C \qquad (4.20)$$

Where $S_K = 1$ when the top switches are gated-ON and $S_K = 0$ when the bottom switches are gated-ON.

4.4.2 Continuous PWM—State Sequence, and Sawtooth Carrier

Table (4.1) lists the fifteen switching states of a three-phase leg source inverter.

Table 4.1 switching states of a three-phase-leg -source inverter

Switches	S1	S2	S3	S4	S5	S6
Active state(finite)	ON	OFF	OFF	OFF	ON	ON
Active state(finite)	ON	ON	ON	OFF	OFF	OFF
Active state(finite)	OFF	OFF	OFF	ON	ON	ON
Active state(finite)	OFF	OFF	ON	ON	ON	OFF
Active state(finite)	OFF	ON	ON	ON	OFF	OFF
Active state(finite)	ON	ON	OFF	OFF	OFF	ON
Zero state (0V)	ON	OFF	ON	OFF	ON	OFF
Zero state(0V)	OFF	ON	OFF	ON	OFF	ON
Shoot-Through-SH1(0V)	ON	OFF	OFF	ON	OFF	OFF
Shoot-Through-SH2(0V)	OFF	OFF	ON	OFF	OFF	ON
Shoot-Through-SH3(0V)	OFF	ON	OFF	OFF	ON	OFF
Shoot-Through-SH4(0V)	ON	OFF	ON	ON	OFF	ON
Shoot-Through-SH5(0V)	ON	ON	OFF	ON	ON	OFF
Shoot-Through-SH6(0V)	OFF	ON	ON	OFF	ON	ON
Shoot-Through-SH7(0V)	ON	ON	ON	ON	ON	ON

In addition to the six active and two null states associated with a conventional VSI, the HPB-QZS inverter has seven shoot-through states representing the short-circuiting of

a phase-leg (shoot-through states SH_1 to SH_3), two phase-legs (shoot-through states SH_4 to SH_6) or all three-phase legs (shoot-through state SH_7). These shoot-through states again boost the DC-link capacitor voltages and can partially supplement the null states within a fixed switching cycle without altering the normalized volt–sec average, since both states similarly short-circuit the inverter three-phase output terminals, producing 0 V across the AC load. Shoot-through states can therefore be inserted to existing PWM state patterns of a conventional VSI to derive different modulation strategies for controlling a three-phase-leg -source inverter.

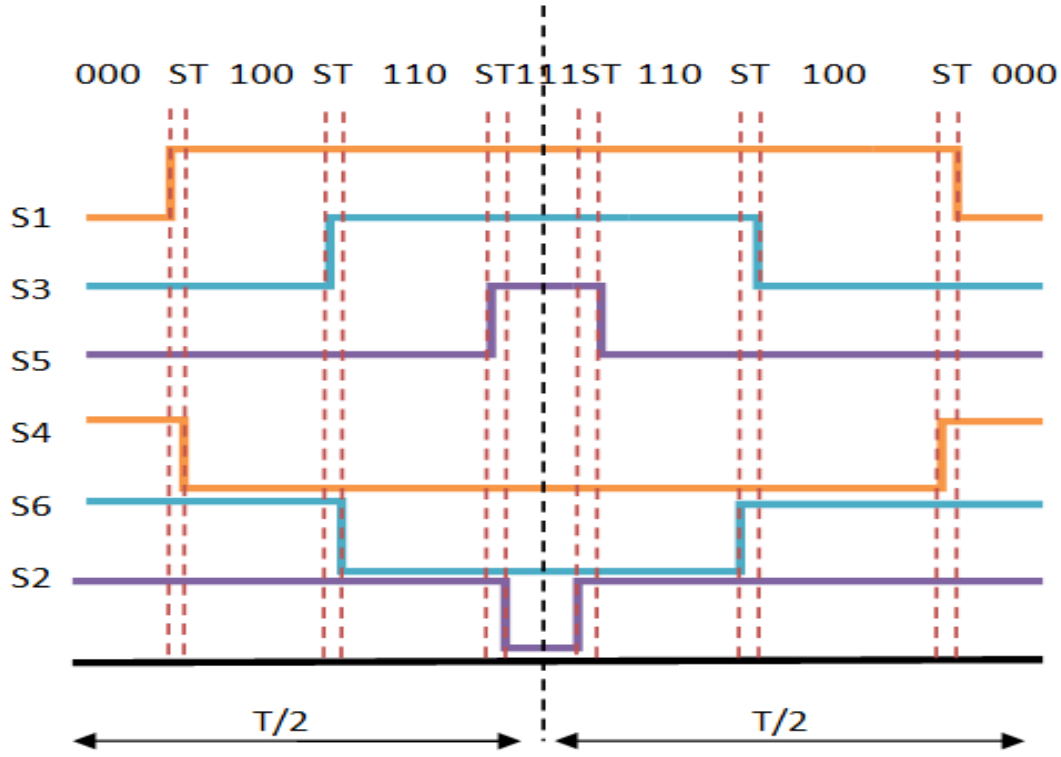


Figure 4.12 shoot-through time period

Figure (4.12) shows shoot-through states can be added immediately adjacent to the active states per switching cycle. The active states {1 0 0} and {1 1 0} are left/right shifted accordingly by $T_0/6$ with their time interval kept constant, and the remaining

two shoot-through states are lastly inserted within the null interval, immediately adjacent to the left of the first state transition and to the right of the second transition. This way of sequencing inverter states also ensures a single device switching at all transitions, and allows the use of only shoot-through states S_1, S_2, and S_3. The other shoot-through states cannot be used since they require the switching of the least two phase-legs at every transition.

4.4.3 Three Phase SPWM Inverter Pulses

This section elaborates on some basic inverter circuit topologies. The square wave and PWM operation are described along with the harmonic spectrum of the output voltages. Sinusoidal pulse width modulation is composed of three sinusoidal waveform with the same amplitude and same frequency where phase shifted by 120^0.The three phase load can be shorted either by having all three top devices or all three bottom devices ON, which they corresponded to zero state because there is no power flow between the DC side and AC side during this state and the load is fully shorted.

4.4.4 Sawtooth comparison PWM

The high frequency carrier-wave is compared with the sinusoidal modulating signals to generate the appropriate gating signals for the inverters. This is one way of generating PWM forms which is the gating signals that requires switching the devices ON or OFF. This method involves comparison of three phase modulating signals.

- Top devices are ON when the modulating signal is greater than the carrier
- Bottom devices are ON when the modulating signal is less than the carrier.

4.4.5 Average voltage in three phase inverter with sinusoidal modulation

The three phase sine wave reference signals are described mathematically as follow:

$$M_R = V_M \, Sin \, \omega t \qquad (4.21)$$

$$M_Y = V_M \, Sin \, (\omega t - 120^0) \qquad (4.22)$$

$$M_B = V_M \, Sin \, (\omega t - 240^0) \qquad (4.23)$$

Where ω is modulation angular frequency which is equal to $2\pi f$, f here is equal to 50Hz.

The M_Y Phase is shifted by 120^0 which is one third of the fundamental cycle and M_B phase modulating signal is the same phase shifted by additional 120^0. M_R, M_Y and M_B are the mathematical description of the three sine wave which can be seen in Figure (4.13).

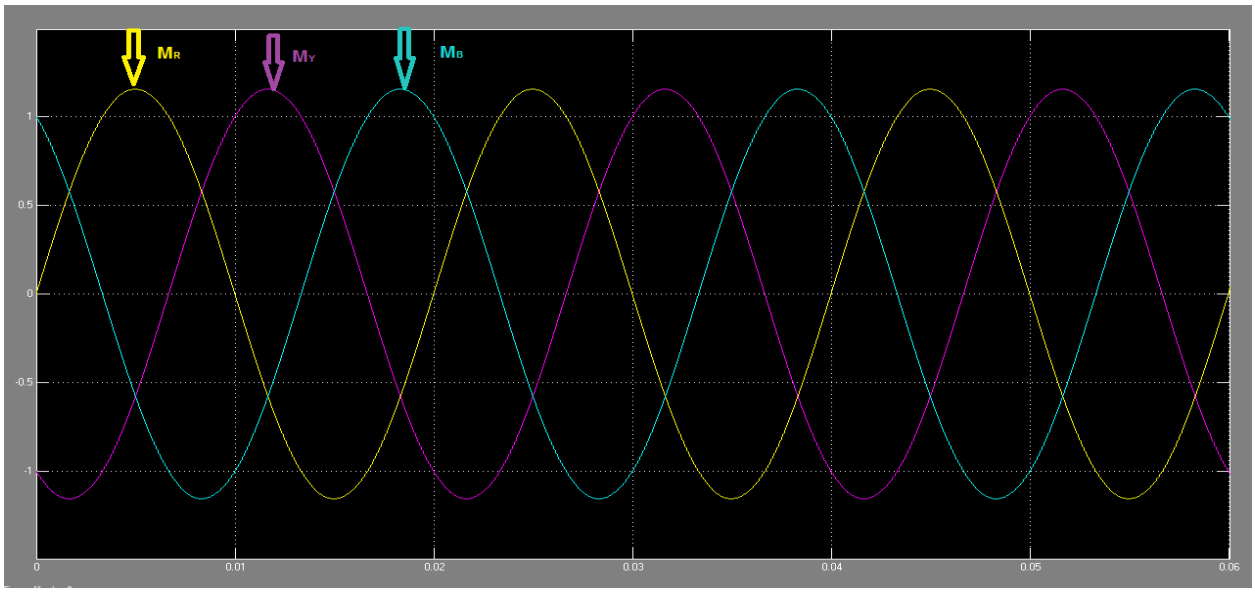


Figure 4.13 Reference signal (three phase sinusoidal waveform)

4.4.5.1 Average pole voltage

Pole is the midpoint of each leg.

$$V_{RO}\ (AV)\ =\ (m_R.V_{dc})/\ (V_P.2) \qquad (4.24)$$

$$V_{YO}\ (AV)\ =\ (m_Y.V_{dc})/\ (V_P.2) \qquad (4.25)$$

$$V_{BO}\ (AV)\ =\ (m_B.V_{dc})/\ (V_P.2) \qquad (4.26)$$

Where the voltage at R is measured with respect to O. And O is the DC bus midpoint. The instantaneous value of V_{RO} if the top device is ON then V_{RO} will be equal to $V_{dc}/2$ and when the R bottom devices is ON the instantaneous voltage will be equal to $-V_{dc}/2$. For any value of $-V_P \leq M_R \leq +V_P$, the average voltage value is $-V_{dc}/2 \leq AV \leq +V_{dc}/2$. In DC-AC conversion the voltage at the pole is sinusoidal quantity, $V_{RO}\ (AV)$ is proportional to M_R which M_R is also sinusoidal quantity and, therefore $V_{RO}\ (AV)$ is sinusoidal. M_R And $V_{RO}\ (AV)$ are scaled version of one and another; hence there is scale factor for M_R and $V_{RO}\ (AV)$ which is equal to $\frac{V_{dc}}{2V_P}$, where V_{dc} is the DC-bus voltage and $V_P$is the peak of the sawtooth carrier. This topology uses bipolar carrier so the peaks are $+V_P$ and $-V_P$.

V_{RO}, V_{YO},V_{BO} Are average pole voltages, the instantaneous pole voltage has been averaged over half carrier cycle.

$$V_{RY}\ (AV)\ = V_{RO}\ (AV)\ -\ V_{YO}\ (AV) \qquad (4.27)$$

$V_{RY\,(AV)}$ is the average line to line voltage, the V_{RO} and V_{YO} quantity are both sinusoidal with the same frequency and different phase shifted which the result is going to be another sinusoidal quantity, but its amplitude is root three of the amplitude of $V_{RO}(AV)$.

Assuming three phase star load which N is the neutral point hence if the load is balanced:

$$V_{RN}\,(AV) = (V_{RY}\,(AV) - V_{BR}\,(AV))/3 \qquad (4.28)$$

$$V_{RN}\,(AV) = (V_m Sin\,(\omega t).\,V_{dc})/2V_P = V_{RO}\,(AV) \quad (4.29)$$

As can be seen above in the special case of sinusoidal modulation the average value of V_{RN} is equal to V_{RO}.

4.4.6 Common mode Injection (Third-Harmonic)

The basic three-phase modulation is obtained by applying a bipolar modulation to each of the three legs of the inverter. The modulating signals have to be 120^0 displaced. The phase-to-phase voltage is three levels of PWM signals that do not contain triple harmonics. If the carrier frequency is chosen as a multiple of three, the harmonics at the carrier frequency and at its multiples are absent. In the case of three-phase modulation it is possible to increase the range of linear operation and decrease the switching losses with respect to the single phase case by adding a zero sequence signal to the modulating signals. The zero sequence signals have no influence on the grid due to the fact that the neutral is not connected.

Practically, depending on the form of the zero sequence voltage added to the modulating signal, there are 2 methods of interest. The classical sinusoidal modulation, indicated with SPWM (sinusoidal PWM), has no zero sequence components.

1) 1/6th third harmonic injection

- If the third harmonic is 17% of the fundamental the maximal linear range is obtained.

2) 1/4th third harmonic injection

- If the third harmonic has amplitude if 25% of the fundamental the minimum current harmonic content is achieved.

The optimum percentage third-harmonic component lies between 25% and 28% and, as expected, the minimum loss coincide with the convergence point of the most important harmonic components (D. Grahame Holmes, 2003). The most significant improvements appear at high frequencies with correspondingly high amplitudes, and at low sampling ratios, but the optimal quantity of added third harmonic is almost independent of these factors.

4.4.7 Average voltages in a three phase inverter with 3rd harmonic injection

According to equations (4.21), (4.22), (4.23)

$$M^*_R = M_R + m_{CM} \qquad (4.30)$$

$$M^*_Y = M_Y + m_{CM} \qquad (4.31)$$

$$M^*_B = M_B + m_{CM} \quad (4.32)$$

Where M^*_R, M^*_Y, M^*_B are the three phase modulating signal with 3^{rd} harmonic injection.

Then:

$$V_{RO}\ (AV) = M^*_R . V_{dc}/V_P 2 \quad (4.33)$$

$$V_{YO}\ (AV) = M^*_Y . V_{dc}/V_P 2 \quad (4.34)$$

$$V_{BO}\ (AV) = M^*_B . V_{dc}/V_P 2 \quad (4.35)$$

In this case V_{RO}, V_{YO}, V_{BO} are not sinusoidal any more. Its Sinusoidal signal + Common mode (3rd harmonic) injection.

$$V_{RY}\ (AV) = V_{RO}\ (AV) - V_{YO}\ (AV) \quad (4.36)$$

Here subtracting $V_{RO}\ (AV) - V_{YO}\ (AV)$ essentially is subtracting $M^*_R - M^*_Y$ which the result is sinusoidal as M_R- M_Y and common mode vanishes.

$$V_{RN}\ (AV) = (V_{RY}\ (AV) - V_{BR}\ (AV))/3 \quad (4.37)$$

As the load is balanced the $V_{RN\ (AV)}$ is the same as sinusoidal modulation.

$$V_{RN}\ (AV) = (V_m Sin\ (\omega t).\ V_{dc})/2V_P \neq V_{RO}\ (AV) \quad (4.38)$$

According to (15)

$$V_{RN}\ (AV) \neq V_{RO}\ (AV) \quad (4.39)$$

Where, $V_{RN}\ (AV)$ is sinusoidal and $V_{RO}\ (AV)$ is not sinusoidal.

4.4.8 Third harmonic injection PWMK=1/6

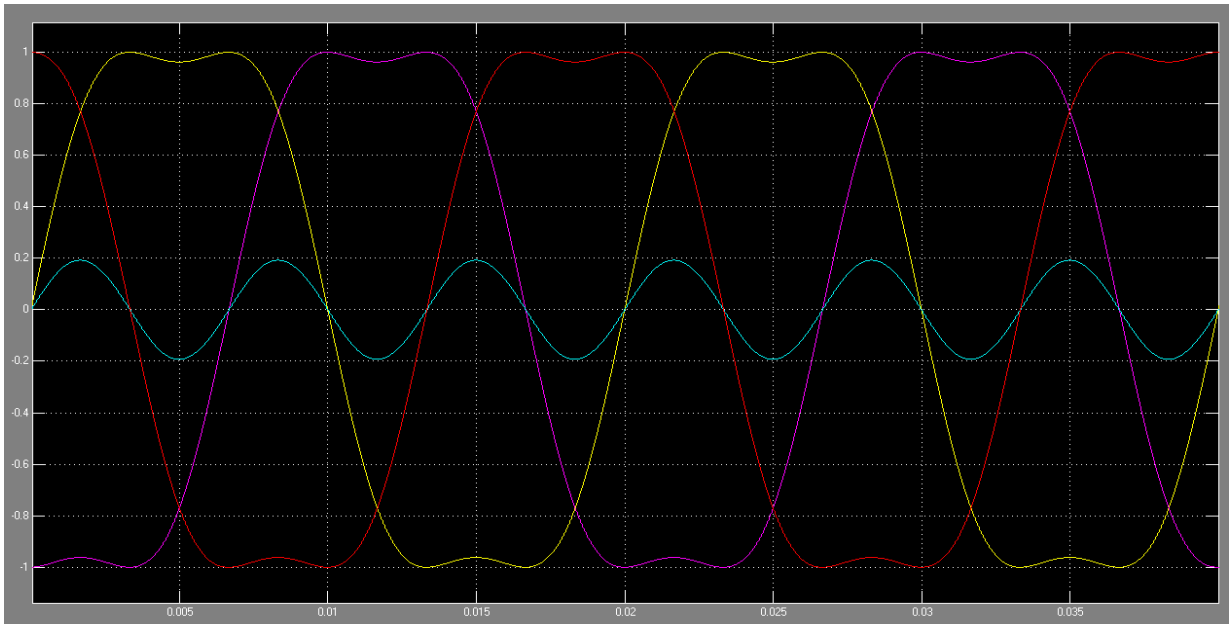


Figure 4.14 Reference signal (1/6 Third harmonic Injection)

According to the sinusoidal modulation (4.13), (4.14), and (4.15) certain common mode (1/6 3rd harmonic) will be added to all the three phase as follow:

$$M^*_R = V_M\, Sin\, \omega t \; + K\, V_M\, Sin\, 3\omega t \qquad (4.40)$$

$$M^*_Y = V_M\, Sin\, (\omega t - 120^0) \; + \; K\, V_M\, Sin\, 3\omega t \qquad (4.41)$$

$$M^*_B = V_M\, Sin\, (\omega t - 240^0) \; + \; K\, V_M\, Sin\, 3\omega t \qquad (4.42)$$

Where, K is the amplitude which is the fraction of V_M. When the $K = 1/6$, can achieve the maximum AC voltage with the given DC voltage.

As can be seen in Figure. (4.13) the original sine wave is set for $2/\sqrt{3}$, so the $V_{Peak} = 1.15$. The original sine wave peak was greater than the peak of the sawtooth

and there was no comparison between the sawtooth carrier and the original sine wave. So the top device always beyond on such kind situation that called over modulation, which introduce lots of distortion in the current because the average pole voltage would not be sinusoidal signal. By comparing the original signal by sawtooth carrier, the average pole voltage cannot go above $V_{DC}/2$ which is the maximum limit. So sinusoidal voltage is applied but the average pole is not sinusoidal. By adding the 3rd harmonic the peak of the modulation signal is 1 and does not go beyond that. By subtracting average pole voltage of R phase with average pole voltage of Y phase the common mode component (3rd harmonic) disappears and the result is a pure sinusoidal waveform without pulse dropping or over modulation. The voltage can be extended up to 15% and $K = 1/6$ it's been found to be the optimal value that gives the maximum line voltage without going to over modulation.

4.4.9 Third harmonic injection K =1/4

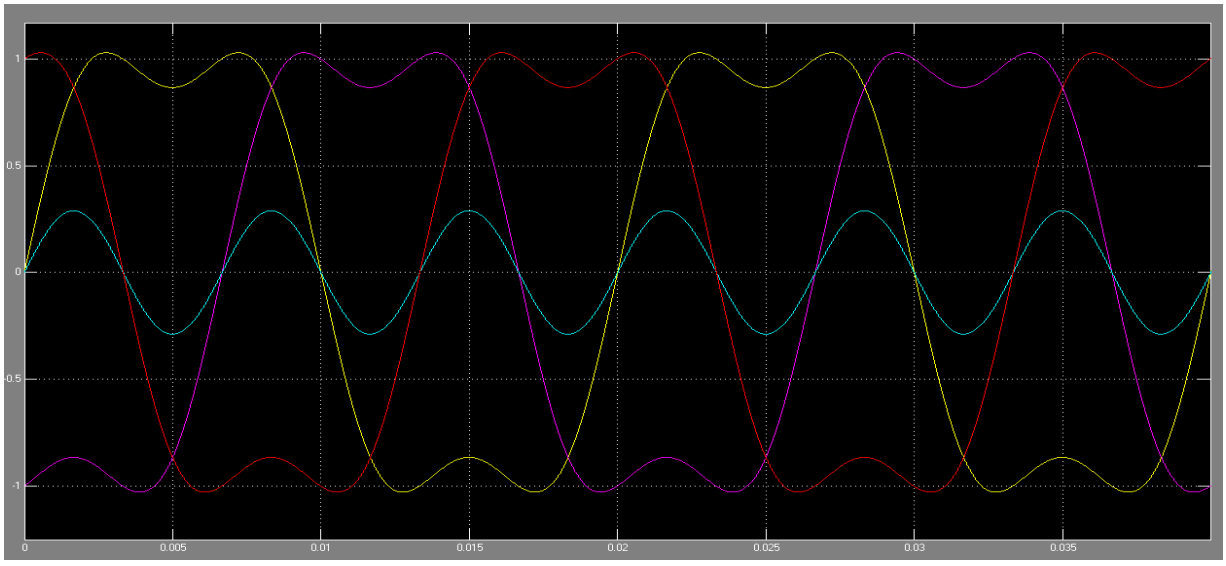


Figure 4.15 Reference signal (1/4 Third harmonic Injection)

Here a quadrant of the amplitude is added. The third harmonic sine wave is ¼ of the amplitude of the original signal. According to Figure (4.14) and (4.15) the difference between the 2 signals are obvious which in 1/6 third harmonic injection the peak head is somewhere close to 60^0 and for ¼ third harmonic injections the peak of the waveform is close to 50^0. The specialty of a quadrant third harmonic is found to be optimal in terms of harmonic distortion. The harmonic distortion and certain amount of RMS current in ripple current is appearing by adding ¼ amplitude of the original signal which in comparison to other values for $k = 1/4$ is lower than $k = 1/6$ .So it has been found to be optimal, which internally make the two zero state equal. In the choice of $K = 1/6$ will give the highest line voltage and for $K = 1/4$ will give the best harmonic distortion. To have an advantage of both, new control strategy is proposed.

$$M^*{}_R = V_M \, Sin\, \omega t + KV_M \, Sin3\omega t \qquad (4.43)$$

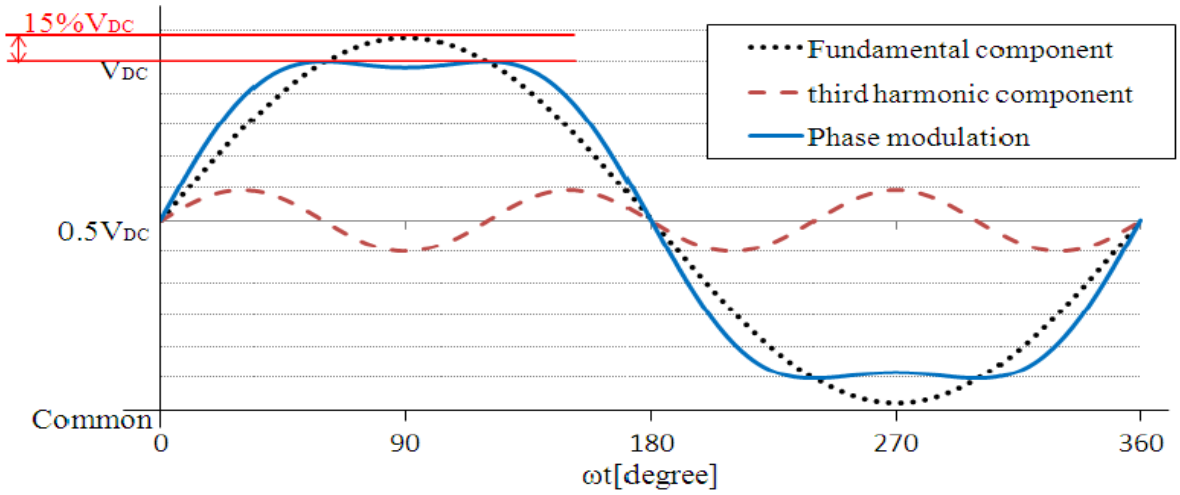


Figure 4.16 third harmonic injection effect

As discussed earlier the waveform peak occurs in different places. According to $K = 1/4$ the peak occurs symmetrically but the angle is occurs in 50^0 which in case of $K = 1/6$ the angle is around 60^0 so where the peak occurs is different [see Figure (4.16)]. To find the K value $(dM^*{}_R)/d_{wt}$ has to be zero, hence can achieve the peak value of ωt. At $M^*{}_R\ \omega t_{Peak}$ the maximum value can be as V_P which shows the maximum possible V_m for the particular value of K. In this case, if the K is equal to $1/6$ the maximum possible V_M is equal to $(2/\sqrt{3})$.

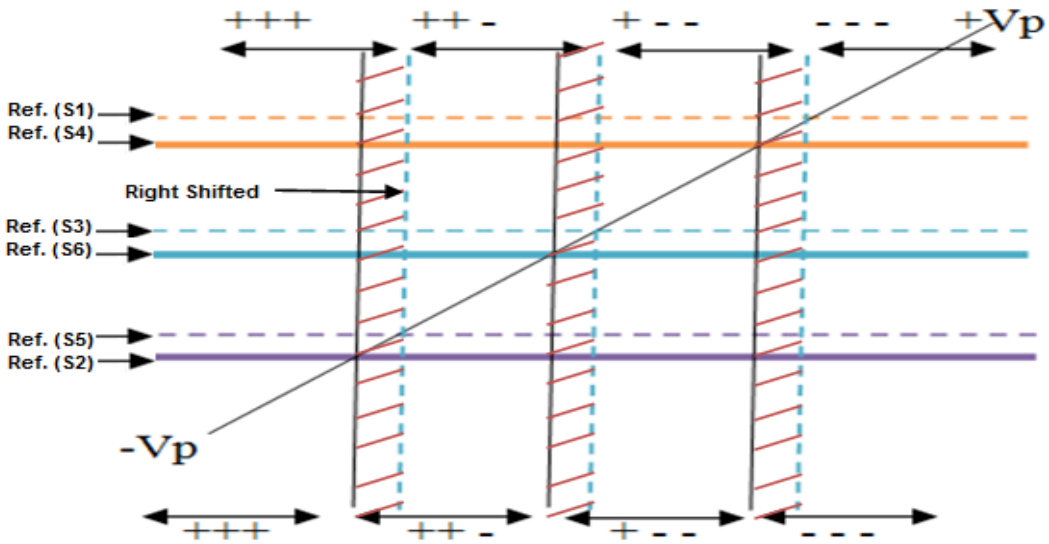


Figure 4.17 Third harmonic injection

Carrier cycle is much smaller than fundamental line cycle, therefore, the sinusoidal signal look almost the straight line; which it looks like a horizontal line, orange line is modulating signal corresponding to Y phase which is sinusoidal signal that appears just as a horizontal line within carrier cycle. So redundancy here is the load that can be shorted either by all top devices being ON or all the bottom devices being ON.

Figure (4.17) shows the extreme situations at the last interval where all the three bottom devices are ON. So in these 2 extreme lines the load is shorted, which is zero state (+ + +), (- - -), and (+ + -) and (+ - -) are active states. By adding common mode signal (3^{rd} harmonic) the switching incident slightly changes. The first intersect with M_B can be seen that shifted to the right. The second intersect is with M_Y which also shifted to the right, but this shifted signal does not make any different to the active mode. The third intersect is with M_R, as we can see all the three switching incident are shifted to the right by the same extent. The effective interval for which the active state is applied, has not changed, but the interval for the zero state has increased.

4.4.10 STC-PWM with 1/6 3rd harmonic injection

In STC-PWM the basic of gate signal generation is the same as conventional system, yet the sawtooth-carrier is used instead of triangular carrier, also common mode ($1/6$ third harmonic) injected to the reference signal.

The gate signals for the switches are shown in table (4.1). The modulation of the HPB-QZSI is different from the H-bridge inverter because of the shoot-through state. The way of adding the shoot through state influences the bidirectional quasi-z-source network design and the system efficiency. In this method, shoot through time period is amalgamated into one-part. In comparison with triangle-carrier, turning ON/OFF of switches is happens once in each period. Hence, improving the efficiency of the system and reducing the switching losses.

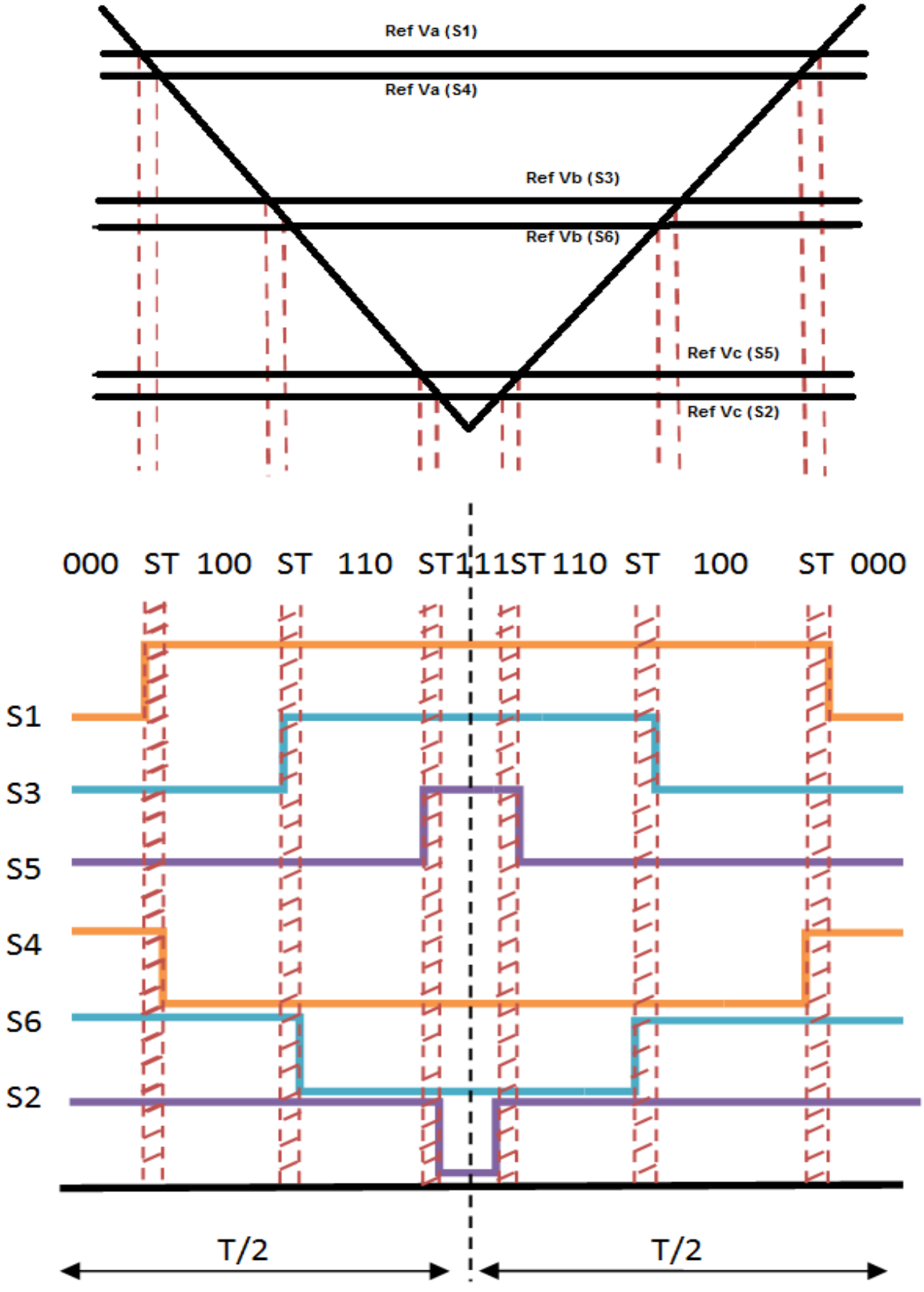


Figure 4.18 Traditional shoot-through insertion

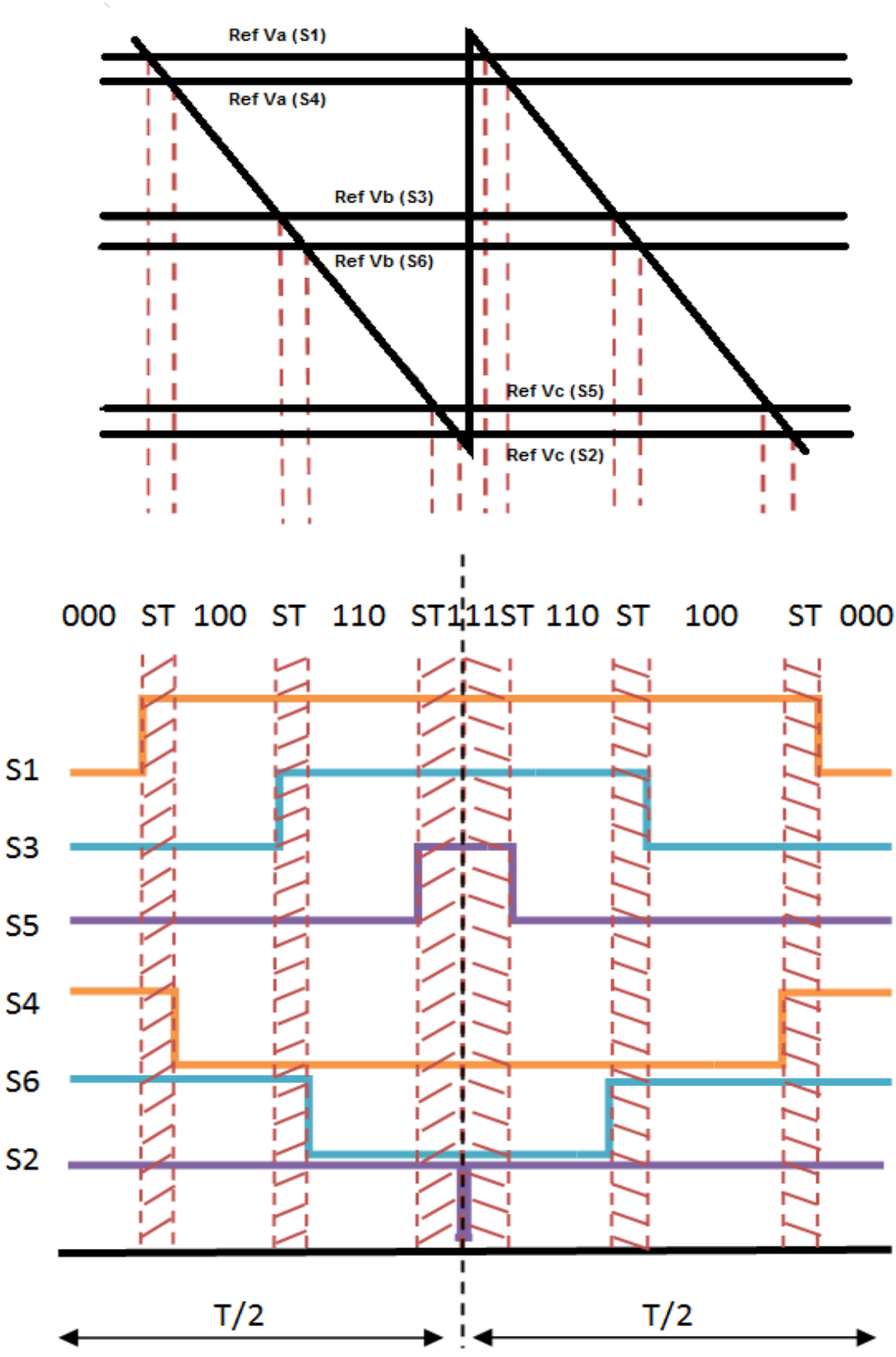


Figure 4.19 New shoot through insertion

The inter-dependency of active state and shoot-through state duty cycle could cause problems in output voltage compensation, and for systems which require independent control of the active and shoot-through states. Every additional shoot-through state increases the commutation time of the semiconductor switches, thereby increasing the switching losses in the system. Therefore, minimization of the commutation time by optimal placing of the shoot-through state in the switching time period is necessary to minimize the switching loss.

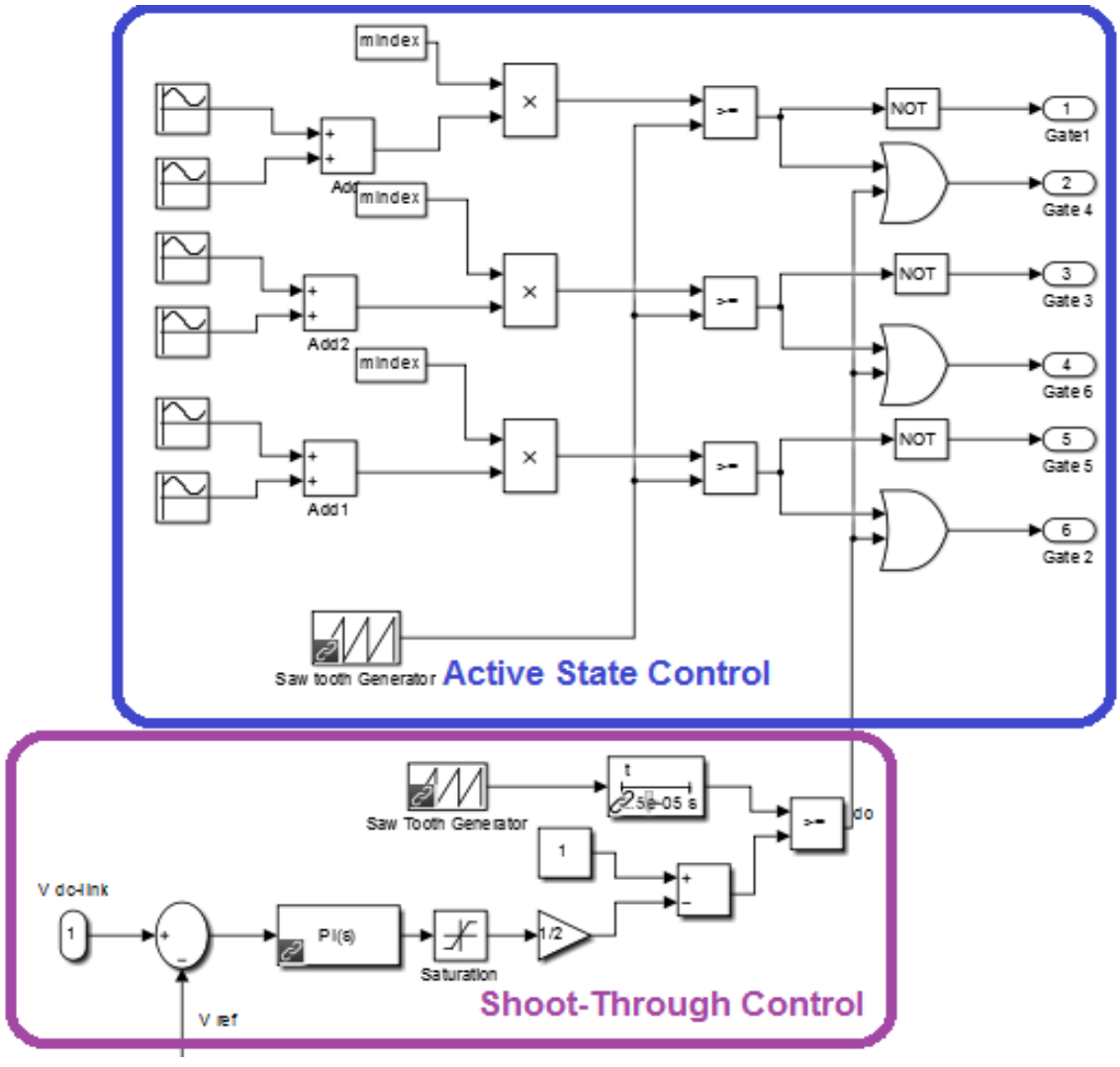


Figure 4.20 block diagram of a circuit to generate the gating signals

Figure (4.20) shows the block diagram of a circuit to generate the gaiting signals by controlling the shoot-through state and active state. In the other control methods modulation index has to be minimum to get the maximum boost factor, but the voltage stress increases with minimum modulation index. This limitation is eliminated in the newly proposed sawtooth carrier PWM with CM injection in direct control system.

The inverter goes through six switching states in one switching period. The active state is kept intact by introducing a shoot through state during the zero state of the switch. This facilitates independent control of active and shoot-through states for output voltage regulation and compensation. The switching signal of the bottom switches is high for $period = T_{SH} + T_A$ (i.e. instead of going low between T_{SH} and T_A), reducing the number of switch commutations compared to traditional shoot-through control methods. The shoot-through state is applied to both sides of the bridge to distribute switch stress during the shoot-through state. The top side switches operate at the switching frequency,fs and the bottom switches at twice the switching frequency $2fs$. The reduction in switch commutations is advantageous compared to conventional techniques (Dmitri Vinnikov, 2013; Roasto et al., 2013) . The PWM signals and the shoot-through signals are generated using a single sawtooth waveform generator and comparing it with the reference signal.

4.4.11 Control strategy for S7

To obtain previous mentioned operation modes, it is significant to control the switch S7. Figure (4.21) shows the drive signal of the $S7$. With the operation modes analysis,

we conclude that switch $S7$ have to operate in off-state during inverter operated in the shoot-through states.

Figure 4.21 switch S7 control strategy

Then, in order to have the required input current ‘in (negative or positive value), which makes the output current ($IL + IC$) of the HPB-QZS network is no less than the load current , the switch $S7$ operate in on-state during the inverter in its non-shoot through states. That is to say, the drive signal of $S7$ is complement with the shoot-through signal as shown in Figure (4.22).

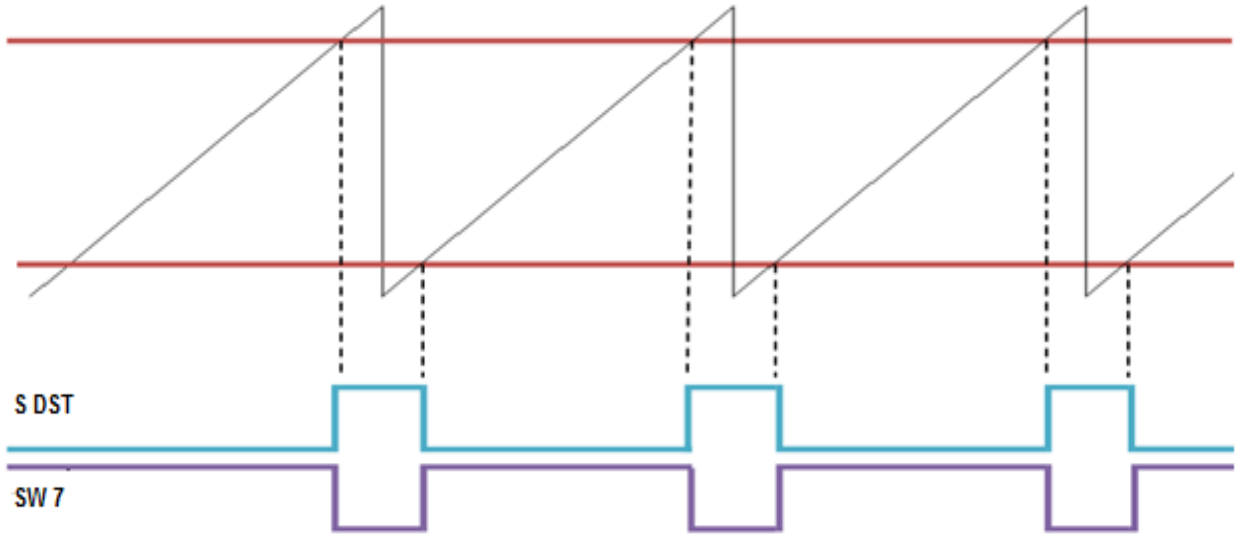


Figure 4.22 the drive signal of switch S7

Chapter 5

Discussions and Critical analysis

5.1 Control-Strategy for DC-Link Boost-Voltage

The control strategy of HPB-QZSI consist of two objectives of controlling the DC and AC side of the HPB-QZSI respectively:

1) Achieving required output AC-voltage by boosting the DC-link voltage when the DC-source output voltage is inadequate.
2) Limited THD content, frequency, output current/voltage quality.

5.1.1The peak DC-link voltage measurement

The DC-link-voltage is a square waveform caused by shoot-through state. The value of DC-link in shoot-through period is zero as this value is in its peak at non-shoot-through period. Hence, controlling the DC-link boost voltage is significantly important as the peak DC-link has to be sensed.(Xinping et al., 2007b) The implementation of sensing and measuring of the peak DC-link is shown in Figure (5.1). Charging the capacitors via diode D by peak DC-link voltage take place when the HPB-QZSI is operating in non-shoot-through period. Whereas the capacitors are discharging via resistors (R1= 10.2 (MΩ), R2=100(kΩ)) slowly, in the shoot-through period. The discharging interval is depends on the component parameters of the whole circuit. The charging and discharging time of the capacitors to a specified voltage needs to be determined.

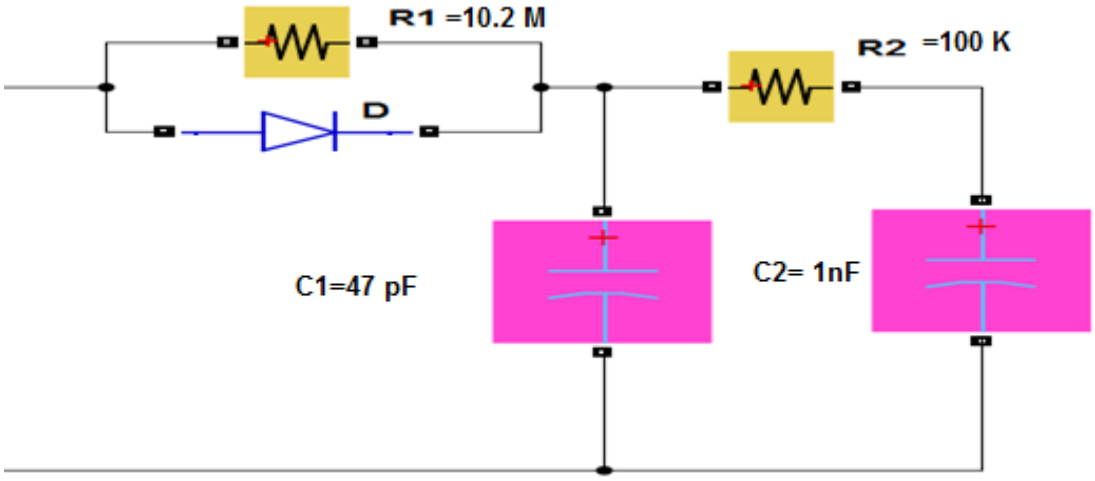


Figure 5.1 Peak DC-link sensing and measuring

Simplified sensing and measuring circuit as shown in Figure (5.2) and Figure (5.3) are in S-domain to derive the time constant for charging/discharging intervals respectively.

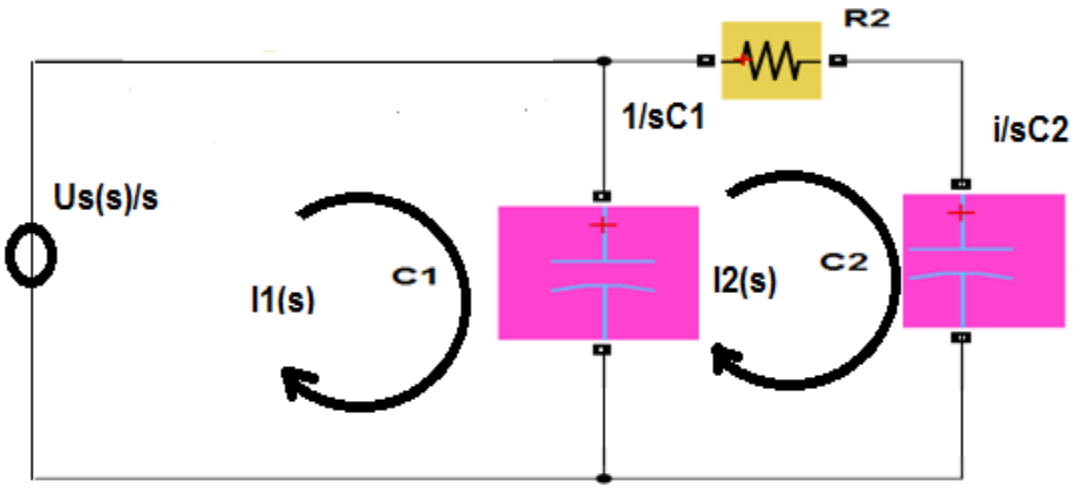


Figure 5.2 Simplified circuit for calculate capacitor charging time constant in S-domain.

Direction of current loop, based on mesh current technique, $I1$ and $I2$ is clockwise (Figure (5.2)). Following equations are based on Kirchhoff voltage law:

$$\frac{us}{s} = \frac{1}{sC1} I1(s) - \frac{1}{sC2} I2(s) \qquad (5.1)$$

$$\left(\frac{1}{sC1} + \frac{1}{sC2} + R2\right) I2(s) - \frac{1}{sC1} I1(s) = 0 \qquad (5.2)$$

With (5.1) and (5.2), one has

$$\frac{us}{s} = (R2C2s + 1)uc(s) \qquad (5.3)$$

Hence, the capacitor voltage response, C2 can be described as:

$$uc(s) = \frac{us}{s} - \frac{us}{\left(\frac{1}{R2C2}\right)+s} \qquad (5.4)$$

In time domain can be written as:

$$uc(t) = us\ \varepsilon(t) - e^{\frac{-t}{R2C2}} us = us\ \varepsilon(t) - e^{\frac{-t}{\tau 2}} us \qquad (5.5)$$

$\tau 2$ is the charging interval time.

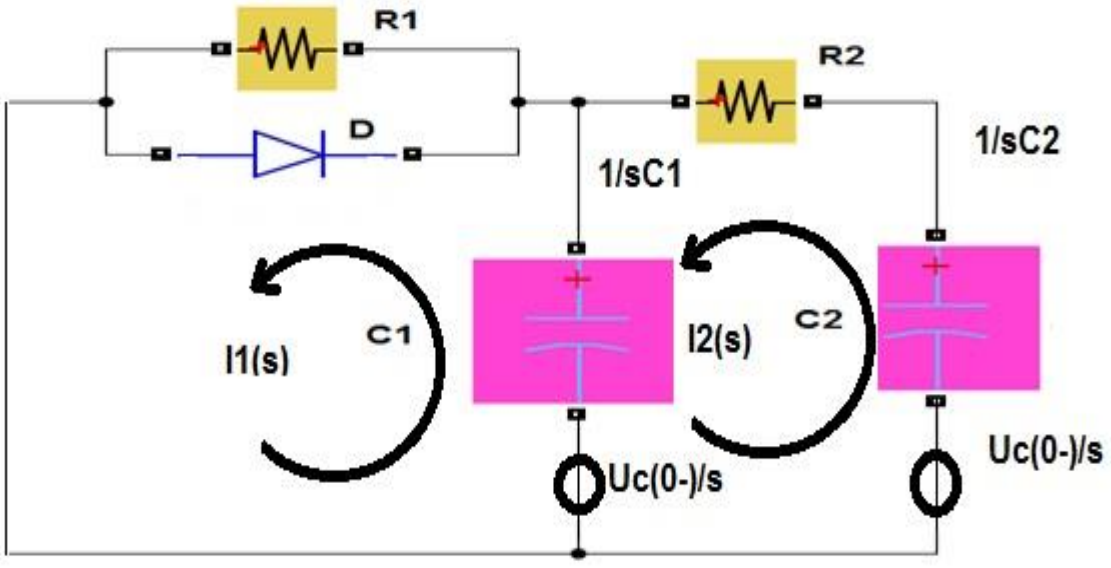


Figure 5.3 Simplified circuit for calculate capacitor discharging time constant in S-domain.

Capacitor C1 and C2 get discharged while the voltage of DC-link is decreasing.

Figure (5.3) shows the sensing and measuring circuit when the DC-link voltage drop to zero.

Assigning the direction of current, $I1$ and $I2$ in anticlockwise is with the aim of simplifying the calculation process. We have:

$$\left(\frac{1}{sC1}+\frac{1}{sC2}+R2\right)I2(s)-\frac{1}{sC1}I1(s)=0 \qquad (5.6)$$

$$\frac{uc(0)}{s}=\left(\frac{1}{sC1}+R1\right)I1(s)-\frac{1}{sC1}I2(s) \qquad (5.7)$$

With (5.6) and (5.7), one has

$$\frac{1}{sC2}I2(s)=\frac{uc(0)}{\tau1\tau2s^2+(\tau1+\tau2+\tau c)s+1} \qquad (5.8)$$

$$uc(s)=\frac{uc(0)}{s}-\frac{1}{sC2}I2(s) \qquad (5.9)$$

$$uc(s)=\frac{uc(0)}{s}-\frac{uc(0)}{s(\tau1\tau2s^2+(\tau1+\tau2+\tau c)s+1)}$$
$$=\frac{\tau1\tau2s+(\tau1+\tau2+\tau c)}{\tau1\tau2s^2+(\tau1+\tau2+\tau c)s+1}uc(0) \qquad (5.10)$$

Where $\tau1$=R_1C_1, $\tau2$=R_2C_2, τc=R_1C_2, uc (0) is the original value of the capacitor C_2 voltage.

We defined $\tau1\tau2=a$, $\tau1+\tau2+\tau c=b$ then the voltage of capacitor C_2 in S-domain can be expressed as:

$$uc(s)=\frac{as+b}{as^2+bs+1}uc(0) \qquad (5.11)$$

In the time domain, it can be expressed as:

$$uc(t) = uc\,(0)(Ae^{\frac{-t}{\tau dis1}} + Be^{\frac{-t}{\tau dis2}}) \qquad (5.12)$$

Where

$$A = (b + \sqrt{b^2 - 4a})/2\sqrt{b^2 - 4a} \qquad (5.13)$$

$$B = -(b - \sqrt{b^2 - 4a})/2\sqrt{b^2 - 4a} \qquad (5.14)$$

$$\tau dis1 = \frac{2a}{b - \sqrt{b^2 - 4a}} \qquad (5.15)$$

$\tau dis1$ is one time constant of discharging interval;

$$\tau dis2 = \frac{2a}{b + \sqrt{b^2 - 4a}} \qquad (5.16)$$

$\tau dis2$ is the other time constant of the discharging interval. The sensing and measuring circuit has specific feature as the time constant for charging is small; $\tau 2 = R_2C_2$ hence, the discharging time constant is larger and almost equal to the switching period.

Table 5.1 parameters of the sensing and measuring circuit(Xinping et al., 2007b)

Parameters	R1(MΩ)	R2(kΩ)	C1(pF)	C2(nF)
Values	10.2	100	47	1

Figure (5.4) and Figure (5.5) shows the effect of two low pass filters before and after zero voltage elimination to obtain the peak DC-link voltage respectively.

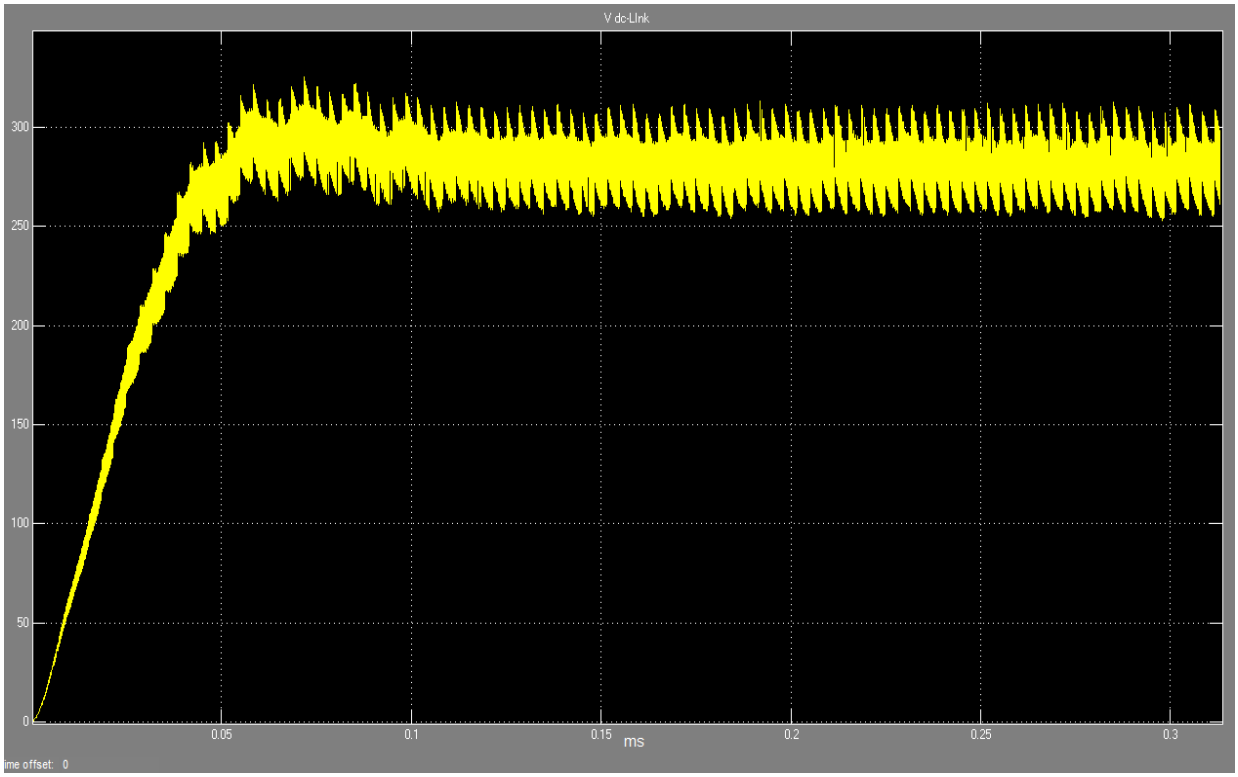


Figure 5.4 before using LPF

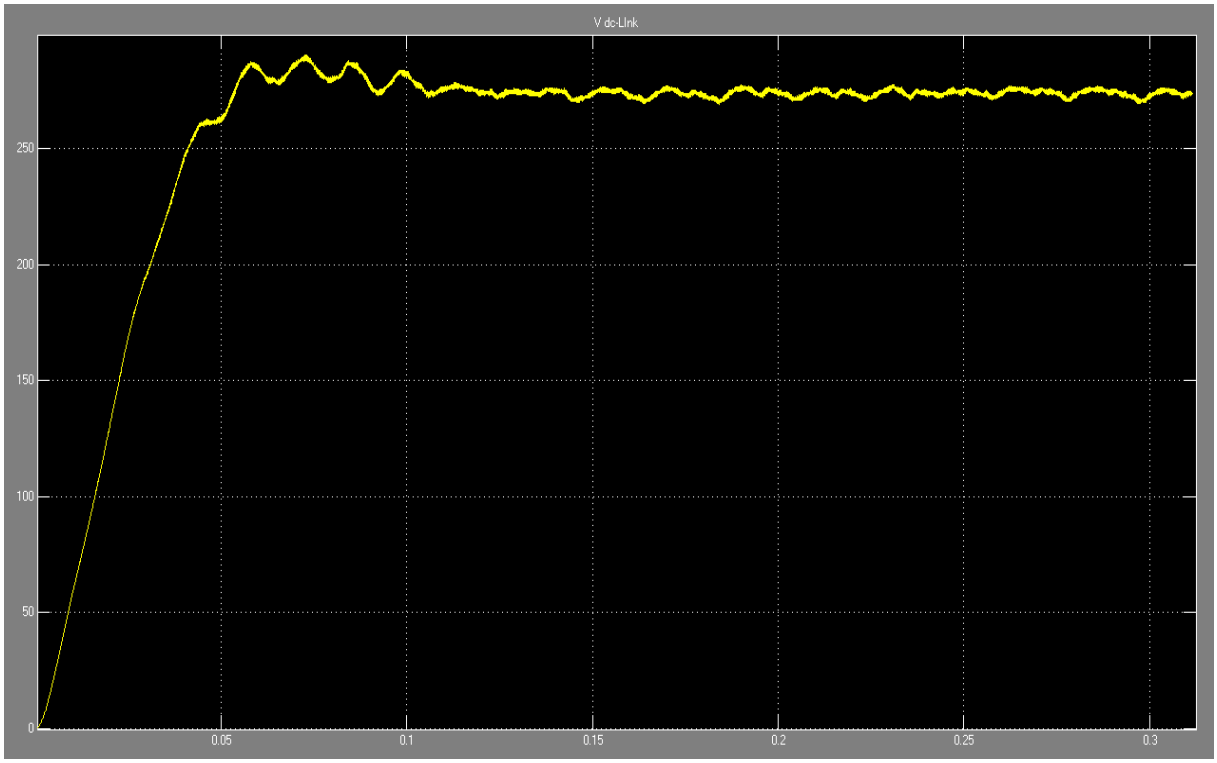


Figure 5.5 peak-DC-link voltage after using LPF

The limitation of impedance source for controlling the DC-link voltage with feedback control is as follows:

A) By inserting the shoot-through time period, the DC-link voltage becomes square, therefore, to control the DC-link in indirect control the capacitor voltage (V_C) is used. [See Figure (3.5)] (Gajanayake et al., 2006; Quang-Vinh et al., 2007).

With shoot-through control is possible to keep the voltage of capacitor V_C constant, nonetheless, during shoot-through regulation peak DC-link voltage will not be controllable any more. By changing the voltage of the source peak DC-link voltage will be changed, but the voltage of capacitor V_C is still the same as before. These effects could be transferred into the output side, which distorts the output voltage, and increases the voltage stress across the switches.

B) The modulation to shoot-through duty cycle transfer function D_o /V_m cannot obtain directly, which increases the difficulty of the compensator design and deteriorate the transient response of DC-link voltage. The peak DC-link voltage direct sensing method is simplifying the controller design, improve the transient response and decrease the voltage stress across the switches.

5.1.2 DC-link Control

High Performance Bidirectional Quasi-Z-source network have been employed to couples the voltage/current source to the converter, load, or another converter. The following can be one or a combination of voltage source: photovoltaic panel, a battery, fuel cell, AC voltage source, diode rectifier, a capacitor, etc. Normally, the buck

operation is accomplished by conventional switching configuration of the converter, where $S1$ is equivalently ON and $S2$ is OFF. None of the inverter phase legs is shorted when it is in OFF state of $S2$. In steady state, we have the output voltage ($V_{C2} = 0v$,$V_{in} = V_{C1} = V_{PN}$) of HPB-QZSI which depends on the switching duty cycle of the conventional converter. By introducing shoot-through states into switch $S2$ (e.g. $S2$ is ON in a short interval $T0$ of one switch duty cycle Ts), a boost operation can be attained. Hence, a switch $S1$ is OFF either due to the active control or circuit (for example a diode is used as $S1$).

The equation for the voltage of the HPB-QZS in steady state can be obtained by defining the shoot-through duty ratio $D_0 = T_0/T_s$ as follows (Anderson and Peng, 2008):

$$v_{C1} = \frac{1-D}{1-2D} v_{in} \qquad (5.17)$$

$$v_{C2} = \frac{D}{1-2D} v_{in} \qquad (5.18)$$

5.2 Small-Signal Model for the HPB-QZSI and Transfer Functions

The main purpose of State Space Averaging (SSA) is to obtain AC small signal model of the HPB-QZSI network in a generalised and more comprehensive way. The following assumptions are made in order to have the simplified model and certifying its lucidity:

1. The IGBTs and diodes are ideal.

2. The load is represented by a current source.

Shoot-through (st)-state and non-shoot-through (nst)-state are two switching states which have taken as basis for applying SSA on the HPB-QZSI. In Figure (5.6), the inverter switches are transformed into the equivalent switch T, which leds to the two switching states on the circuit. (Poh Chiang et al., 2007d; Gajanayake et al., 2007; Yuan et al., 2013) have proven the feasibility of this approach.

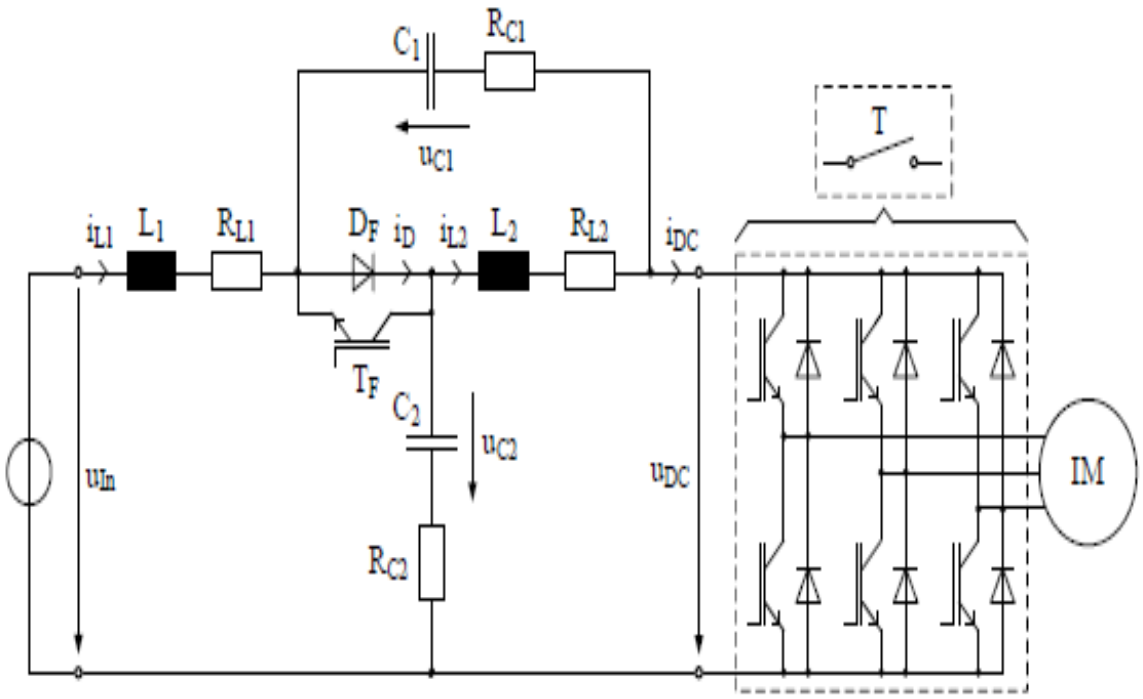


Figure 5.6 HPB-QZSI coupled to an induction machine

On the basis of DC-AC conversion, the ac small-signal modelling and analysis is established. In addition to this, other forms of conversion such as DC-DC converter or AC-DC converter, for the DC side modelling can be represented by the single switch S_2 and current source connected in parallel (Jingbo et al., 2007; Gajanayake et al., 2007).

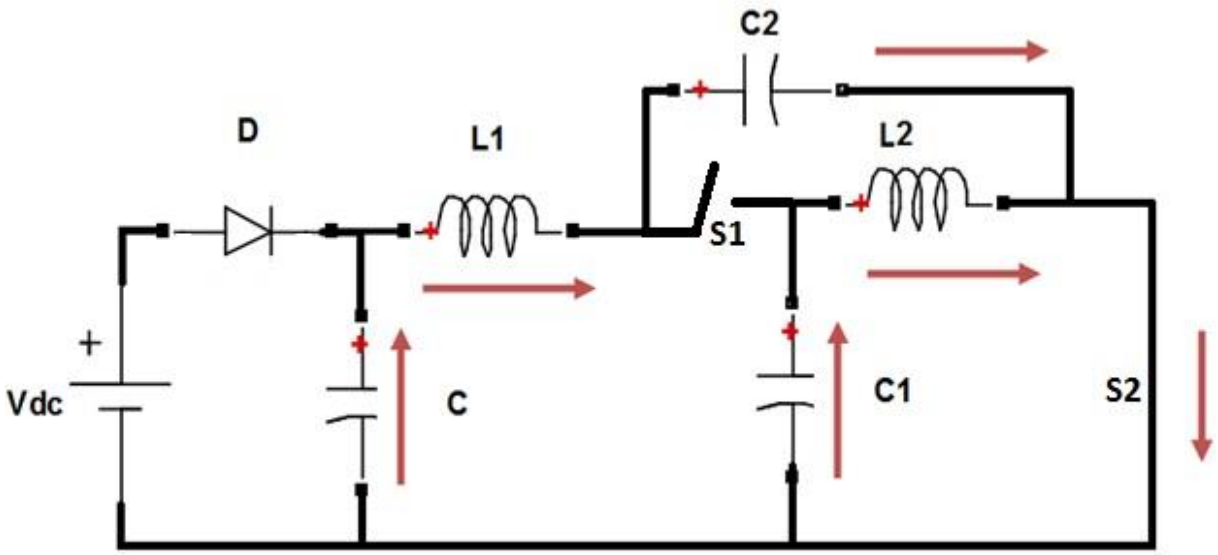


Figure 5.7 Equivalent circuit of the HPB-QZS network

Figure (5.7) represents the equivalent circuit of the HPB-QZS network in shoot-through state which S_2 is ON and the load is shorted by the converter bridge. Input voltage V_{in} considered to be as one system input. Given the fact that the real source such as PV panels or fuel cells doesn't consist of stiff output characteristics as compared to an ideal voltage source in many applications, one function of V_{in}can be determined by the input current i_{in}, which in turn specified by the energy source nature.

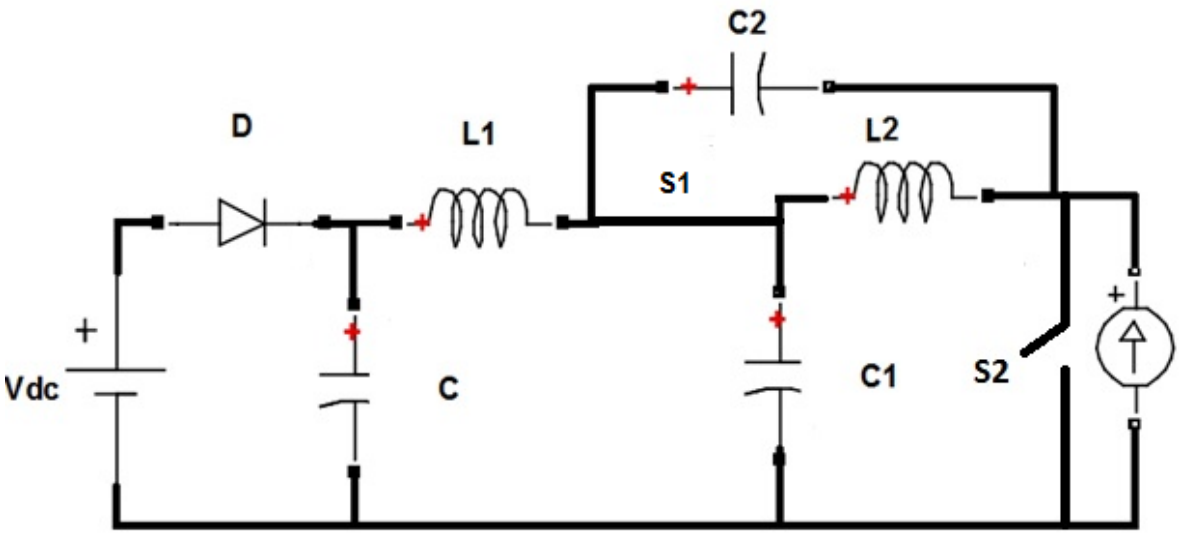


Figure 5.8 equivalent circuit for HPB-QZS network in non-shoot-through

The corresponding circuit of the HPB-QZS network in non-shoot-through state can be visualised in Figure (5.8).in which the load current i_{Load}flow through the HPB-QZSI and S_2 is in OFF state. The current through two inductors i_{L1} ,i_{L2}; the voltage across the capacitors V_{C1} , V_{C2}; are the four state variables in the asymmetric HPB-QZS network.

Another input (disturbance) of the HPB-QZS network is served by the load current i_{Load}. To simplify the analysis, according to Figure (5.6) assume that the stray resistances of inductors $R_L = R_{L1} = R_{L2}$, the equivalent series resistances (ESR) of capacitors $R_C = R_{C1} = R_{C2}$ and $C = C_1 = C_2, L = L_1 = L_2$. Capacitors transfer their electrostatic energy to magnetic energy stored in inductors at the shoot-through state as shown in Figure (5.6). The equations for the dynamic state of the quasi-Z-source network are given as:

$$\dot{x} = A_{st}\, x + B_{st}\, u \qquad (5.19)$$

$$\begin{bmatrix} \acute{i}_{L1} \\ \acute{i}_{L2} \\ \acute{u}_{C1} \\ \acute{u}_{C2} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+R_C)}{L} & 0 & 0 & \frac{1}{L} \\ 0 & \frac{-(R_L+R_C)}{L} & \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_{in} \\ i_{Load} \end{bmatrix} \qquad (5.20)$$

In Figure (5.7), the DC power source including inductors charges capacitors and powers the external AC load at the non-shoot-through states; boosts the DC voltage across the inverter bridge. The equations for the dynamic state are shown as:

$$\underbrace{\dot{x}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{-(R_L+R_C)}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & \frac{-(R_L+R_C)}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}}_{A_{non\text{-}st}} \underbrace{\begin{bmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} & \frac{R}{L} \\ 0 & \frac{R}{L} \\ 0 & -\frac{1}{C} \\ 0 & -\frac{1}{C} \end{bmatrix}}_{B_{non\text{-}st}} \underbrace{\begin{bmatrix} u_{in} \\ i_{Load} \end{bmatrix}}_{u} \quad (5.21)$$

Perturbations $\hat{v}_{in}(t)$ and $\hat{d}(t)$ are added to the input voltage and the duty ratio in order to derive the small signal model (Erickson, 2001).The State Space Average method is formulated as:

$$\dot{x} = (D.A_{st} + (1-D).A_{nst})\,\dot{x} + (D.B_{st} + (1-D).B_{nst})\,\dot{v} + ((A_{st} - A_{nst}).x + (B_{st} - B_{nst}).u).d'(t) \quad (5.22)$$

After the application of Laplace transformation, it becomes:

$$\begin{aligned} sL1 \cdot \hat{i}_{L1}(s) &= -(1\text{-}D) \cdot \hat{v}_{C1}(s) + D \cdot \hat{v}_{C2}(s) + \hat{v}_{in}(s) + (V_{C1} + V_{C2}) \cdot \hat{d}(s) \\ sL2 \cdot \hat{i}_{L2}(s) &= D \cdot \hat{v}_{C1}(s) - (1\text{-}D) \cdot \hat{v}_{C2}(s) + (V_{C1} + V_{C2}) \cdot \hat{d}(s) \\ sC1 \cdot \hat{v}_{C1}(s) &= (1\text{-}D) \cdot \hat{i}_{L1}(s) - D \cdot \hat{i}_{L2}(s) - (1\text{-}D) \cdot \hat{i}_{l}(s) + (I_l - I_{L1} - I_{L2}) \cdot \hat{d}(s) \\ sC2 \cdot \hat{v}_{C2}(s) &= -D \cdot \hat{i}_{L1}(s) + (1\text{-}D) \cdot \hat{i}_{L2}(s) - (1\text{-}D) \cdot \hat{i}_{l}(s) + (I_l - I_{L1} - I_{L2}) \cdot \hat{d}(s) \end{aligned} \quad (5.23)$$

The small signal model of the HPB-QZSI is formed by the set of equations in (5.23). Analysis results based on (5.23) are compared with detailed circuit simulation results in order to validate the derived small signal model. Assuming that the two HPB-QZS inductors have the same inductance *L* and the two capacitors have the same capacitance *C*, the circuit parameters used in the study:

Input Voltage: 140V, Inductance in HPB-QZSI: 500 μH, Capacitance in HPB-QZSI: 400 μF, Load Resistance: 2Ω , Load Inductance: 24 μH , Switching Frequency: 10 KHz.

Figure (5.9) plots the analysis and simulation results from both small signal model and detailed circuit model, includes of, 20-V disturbance from the input voltage is introduced to the system, the response of the capacitor voltage v_{C1}, and the response of the inductor current i_{L1}.

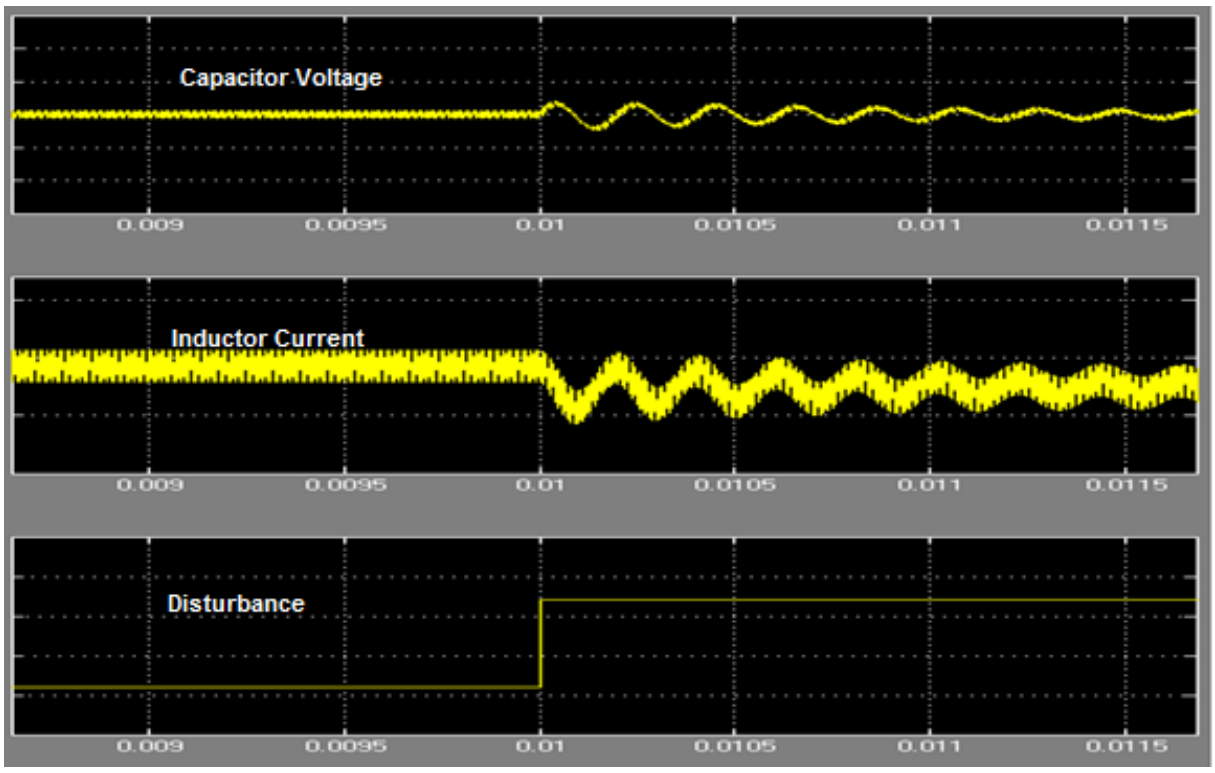


Figure 5.9 step response

From this, we can easily visualise that the values from the small signal model based analysis are in line with the detailed circuit simulation results. Hence, (Jingbo et al., 2007; Erickson, 2001; Krein et al., 1990) verifies the small signal model. At the switching frequency, the high frequency ripple is presented in the detailed circuit model. Beside this, a constant oscillation in the system is found after introducing the disturbance. An inherent characteristics of the HPB-QZSI is discussed in the next section.

5.2.1 DC Side Controller Design

In (5.23), we have in total four equations, two perturbation variables and four state variables. In this way, we can express the response of each state variable as a linear combination of two perturbation variables by solving (5.23) as follows:

$$G_{vdc} = \frac{L_l L(I_l - I_{L2} - I_{L1}).s^2 + [(1-D).(LV_{C1} + LV_{C2}) + R_l.L(I_l - I_{L2} - I_{L1}) + L_l.V_{in}].s + V_{in}.R_l}{L_l.LC.s^3 + R_l LC.s^2 + [L_l(1-2D)^2 + 2L(1-D)^2].s + (1-2D)^2 R_l} \quad (5.24)$$

Equation (5.24) is the control to output transfer function of HPB-QZSI. In Figure (5.10), the pole-zero maps of the transfer function $G_{vdc}\ (s)$ is plotted. It can be noticed that there is a right-half-plane (RHP) zero in the transfer function $G_{vdc}\ (s)$ that indicates the system is a non-minimum-phase system. Because of this RHP zero, the system dynamic response may be limited. However, the DC side controller is usually designed to be much slower than the AC side controller to avoid oscillation.

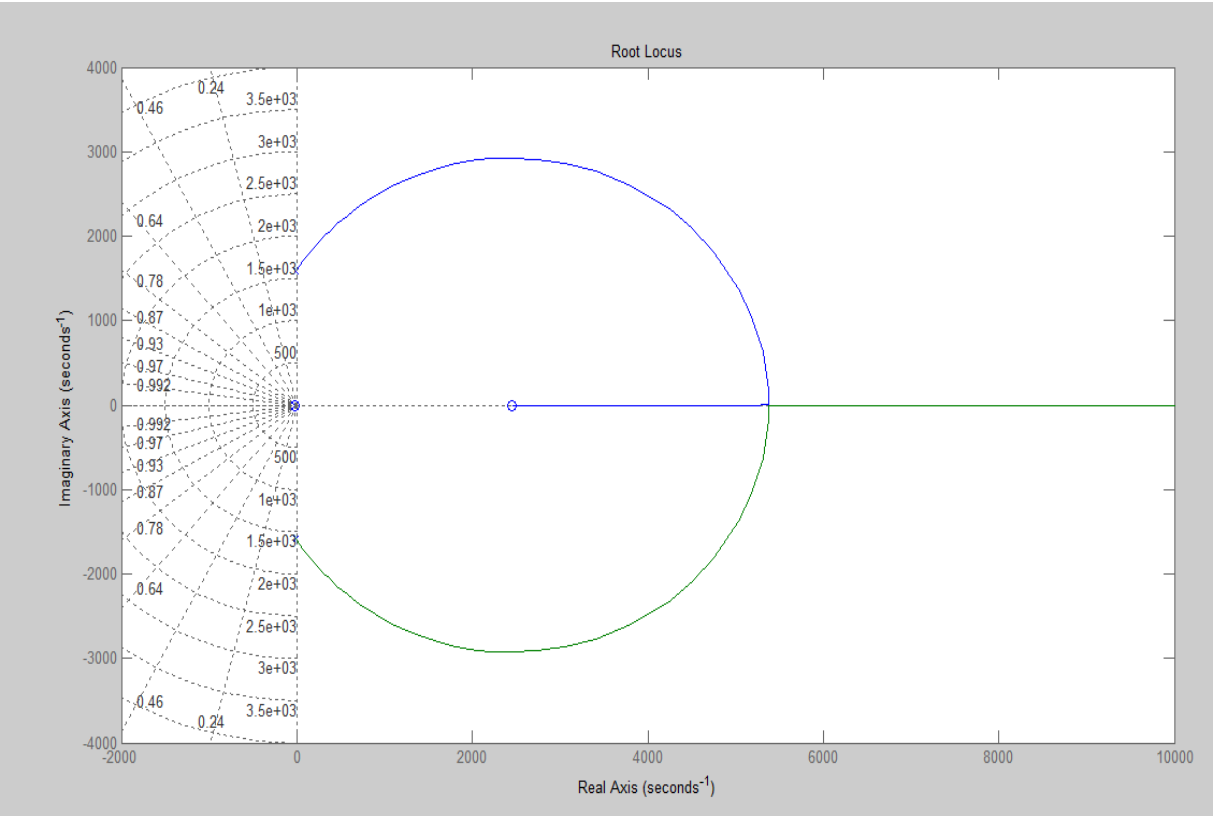


Figure 5.10 Pole-Zero map of the transfer function G_{vDC}

As an application of the small signal modelling of the HPB-QZSI this subsection presents a way to control the HPB-QZSI to operate in stand-alone mode. The system does not have enough damping to suppress the disturbance from the input voltage .To realise the DC-link voltage control, a dedicated voltage controller with feed-forward compensation is proposed. The reference value of $V_{DC\text{-}link}$ can be measured based on the previous analysis and by feeding back the DC-link voltage to the controller can stabilise the DC-link voltage to the reference value. In addition to this, the performance of the input voltage disturbance rejection can be greatly improved with this approach. The simplified DC side control diagram is illustrated in Figure (5.11).

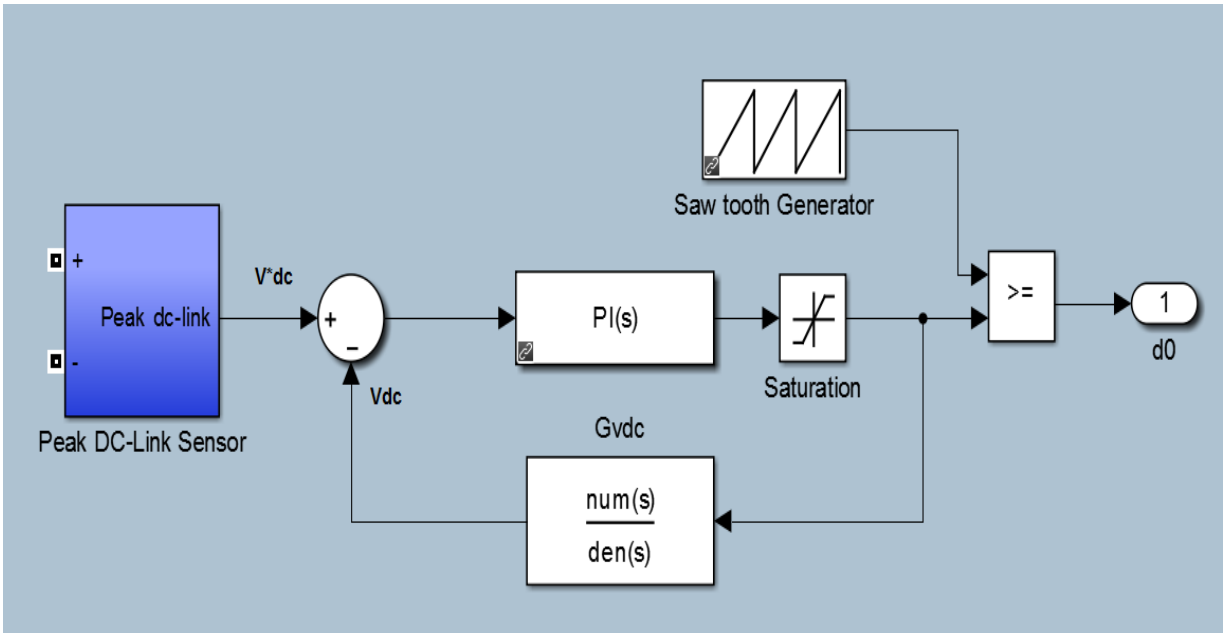


Figure 5.11 DC-side control diagram

The following transfer function described a proportional-integral (PI) controller which is used in the control loop:

$$\text{PI}= K_P.(1+\frac{K_i}{s}) \qquad (5.25)$$

5.2.2 Dynamic Characteristics of the HPB-QZS Network

The characteristic equation of the HPB-QZS network can be obtained as (5.26).

$$s^2+\frac{R_c+R_L}{L}s+\frac{(1-2D)^2}{LC}=0 \qquad (5.26)$$

The normalised form of equation (5.26) is:

$$s^2+2\xi\omega_n s+\omega_n^2=0 \qquad (5.27)$$

And, the natural frequency is

$$\omega_n=\frac{1-2D}{\sqrt{LC}} \qquad (5.28)$$

Also, the damping ratio is

$$\xi = \frac{R_C + R_L}{2(1-2D)}\sqrt{\frac{C}{L}} \qquad (5.29)$$

The characteristic equation clearly indicates that (D) has an effect on dynamic characteristics of the system as well as passive components. From equation (5.29), by increasing C damping ratio would increase and by increasing L damping ratio will be decreased.

Figure (5.12) shows the bode plot for reference tracking of the control to output transfer function after compensation which demonstrates the function of the proposed controller.

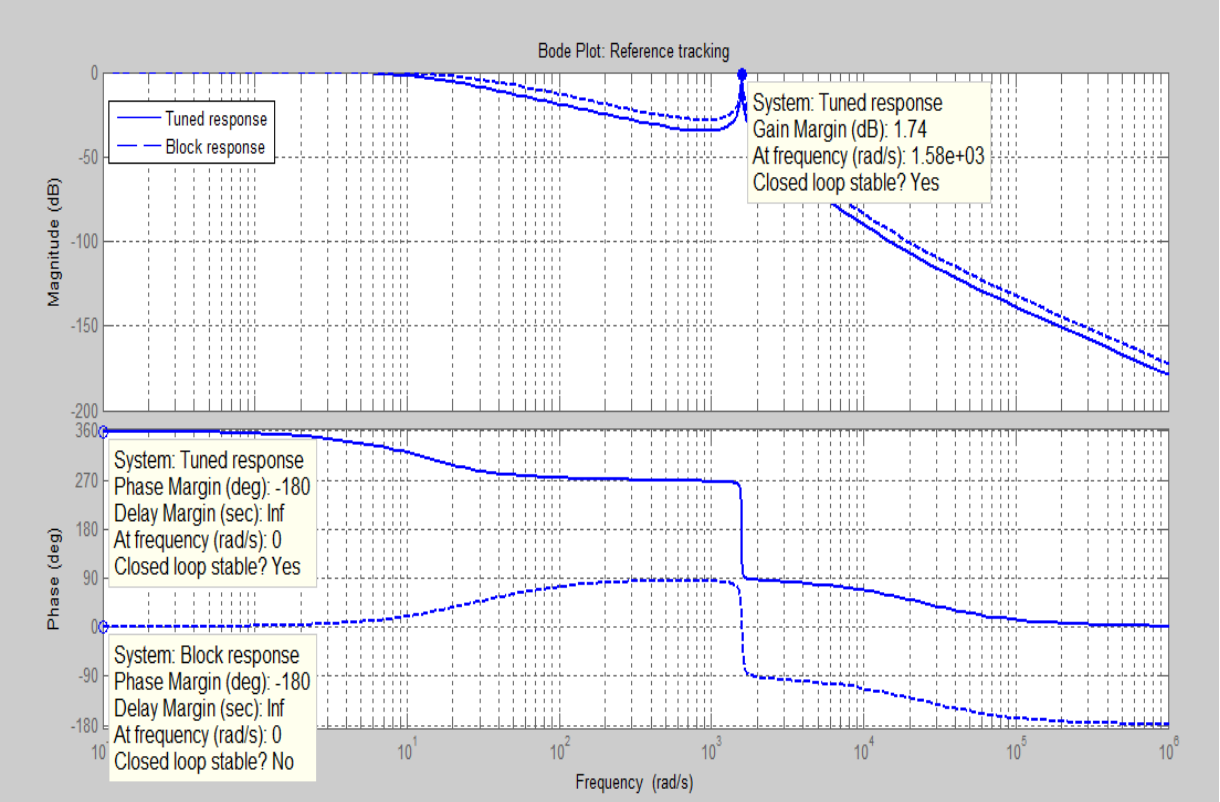


Figure 5.12 Bode plot- reference tracking

For the AC-side control, traditional methods explored for voltage regulation are applicable for the stand-alone system. To achieve a good system level control, the dynamics of the ac side should be designed to be much faster than the DC side to avoid oscillation. Since the shoot-through state is always restricted within the zero state (Fang Zheng et al., 2005b), the change of the control parameter at the DC side will impose limitation on the ac side. With a higher input voltage, to achieve the same DC-link voltage, the required shoot-through duty ratio will be smaller. Therefore, there will be less possibility that the DC side shoot-through duty ratio controller conflicts with the ac side controller. So the controller usually will perform better with higher end of input voltage range. In three-phase system, fundamental frequency components are commonly transformed to DC components via d-q transformation, where simple PI compensator can be applied with good performance. Another choice is to design the controller in stationary frame. Without d-q transformation, the designed controller is applicable to single-phase system too. A typical multi-loop controller in stationary frame as the voltage regulator (Yuan et al., 2010; Abdel-Rahim and Quaicoe, 1996) can be seen in Figure (5.13).

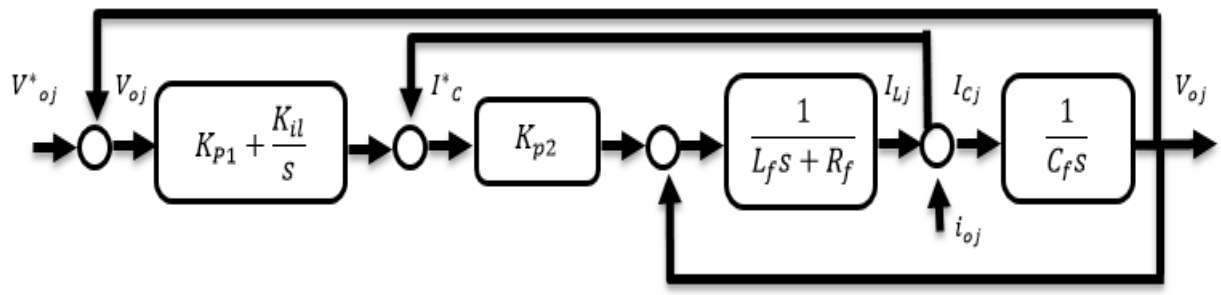


Figure 5.13 AC control loop

The controller consists of inner current loop and outer voltage loop. A faster response and stabilized output for a current disturbance is obtained via proportional compensator which is used with the inner current loop. PI compensator is used with the outer voltage loop that gives the stabilized slower variations and a good reference tracking. The closed-loop transfer functions by applying the Mason's gain rule can be obtained as follows:

$$G_{iCj^*}^{iCj}(s)=\frac{i_{Cj}(s)}{i^*_{Cj}(s)}=\frac{K_{P2}C_f s}{L_f C_f s^2+(R_f+K_{P2})C_f s+1} \quad (5.30)$$

$$G_{ioj}^{iCj}(s)=\frac{i_{Cj}(s)}{i_{Cj}(s)}=-\frac{L_f C_f s^2+R_f s}{L_f C_f s^2+(R_f+K_{P2})C_f s+1} \quad (5.31)$$

$$G_{voj^*}^{voj}(s)=\frac{v_{oj}(s)}{voj^*(s)}=\frac{(K_{P1}+K_{il})K_{P2}}{L_f C_f s^3+(R_f+K_{P2})C_f s^2+(1+K_{P2}K_{P1})s+K_{il}K_{P2}} \quad (5.32)$$

$$G_{i_{oj}}^{voj}(s)=\frac{v_{oj}(s)}{voj^*(s)}=-\frac{L_f s^2+R_f s}{L_f C_f s^3+(R_f+K_{P2})C_f s^2+(1+K_{P2}K_{P1})s+K_{il}K_{P2}} \quad (5.33)$$

Where $G_{iCj^*}^{iCj}(s)$ and $G_{ioj}^{iCj}(s)$ are the transfer function of control-to-output, disturbance-to-output of inner current loop, respectively; $G_{voj^*}^{voj}(s)$ and $G_{i_{oj}}^{voj}(s)$ are the transfer functions of control-to-output, disturbance-to-output of outer voltage loop, respectively; K_{P2}, K_{P1}, K_{il} are control parameters.

5.3 Summary

This chapter has emphasized a direct control method for the HPB-QZSI. The dynamical characteristics of the HPB-QZSI network have been investigated through small-signal analysis. Based on the dynamical model, the direct control method for HPB-QZSI operating in both output voltage control and current control modes, has

been presented. The voltage stress in the proposed control method is much lower, which means, for given devices, the inverter can be operated to obtain a higher voltage gain. In addition, the switches achieve zero voltage switching (ZVS) which reduce EMI and improves efficiency of the inverter.

The following points should be considered while placing the shoot-through state in the PWM control system for a HPB-QZSI:

1) The maximum shoot-through duty cycle should never exceed 0.5, otherwise the system gets unstable.

2) The minimum number of shoot through states per switching period is three. One shoot-through state per period causes a discontinuous current and the converter will behave abnormally.

3) The shoot-through state should be in the zero state, i.e. the intact active state.

4) The active state and the shoot-through state should be independently controllable.

Chapter 6

Validation and Simulink Results

6.1 Introduction

Traditionally two approaches are used to simulate power electronic systems:

The first, so called fixed topology, where semiconductors are impedances with low or high values based on their ON-state or OFF-state respectively. System equations does not depend on the state of the semiconductor. Despite its simplicity, this approach raises problems of compromise between accuracy of the results and stability of numerical integration methods.

The second, so called variable topology, assimilates the switches to open-circuits or short-circuits (ideal switches). The system equations then depend on the state of the semiconductor. There are no accuracy problems but writing the equations of different configuration can be laborious as well as obtain switching conditions of the semiconductor. This chapter proposes a method for simulating inverter with Simulink based on the variable loads where switching conditions of semiconductor are realised by switching functions.

The components constituting an Inverter are:

- Capacitors and inductors

- Power semiconductors, IGBT operating as switches

The design of power converter consumes time with a significant cost. Performance is generally determined after testing inverters at nominal operating points. Thus, simulation can substantially reduce development cost. The development of specific software dedicated to simulation of power electronic systems (PSIM, SABER, PSCAD, “SimPowerSystems” toolbox of Simulink…) allows simulating fast and accurately the converter behaviour. “Unfortunately, the designers of converters don’t always have such available software. In many cases, they have to simulate power electronics devices for occasional need. So they don't want to buy the SimPowerSystems toolbox in addition to Matlab and Simulink”. The purpose of this chapter is to present the ability to simulate power converters using only Simulink. Simulink is a graphical extension to Matlab for representing mathematical functions and systems in the form of block diagram, and simulate the operation of these systems.

6.2 DC-AC inverter model in Simulink

This part will be dedicated to the DC-AC inverter modelling with Simulink. The input generator is a DC voltage source and the output generator is AC voltage. For general analysis purposes, input voltage V_{in} is chosen as system input, to which input current I_{in} is related. This is because Renewable Energy Sources (RES) does not have as stiff output characteristics as an ideal voltage source or current source.

The new modulation and control technique presented in previous chapter; maximum boost with controllable shoot through insertion have been simulated using Simulink-Matlab for HPB-QZS network. The aim of comprehensive simulation was a

detailed comparison of HPB-QZSI feature under various loads. All components are assumed to be ideal in character. The initial voltage for capacitor is 0 V.

Four different loads are connected at the output of the HPB-QZSI:

Induction machine of 10 kW and 0.3 kVar from 0 to 0.2 s.

The R-L load of 8 kW and 0.30 kVar applied from 0.2 to 0.3 s

The R-L load of 8.5 kW and 0.30 kVar applied from 0.3 to 0.4 s

Induction machine of 7.5 kW and 0.3 kVar from 0 to 0.4 s

The circuit parameters are $L1 = L2 = 1mH, C1 = C2 = 1000\mu F, Lf = 1\ mH,\ Cf = 50\mu F,\ Vin = 140V, d0 = 0.30$, and the carrier frequency is kept at 10 KHz.

6.3 Three Loads applied from 0 to 0.4 s

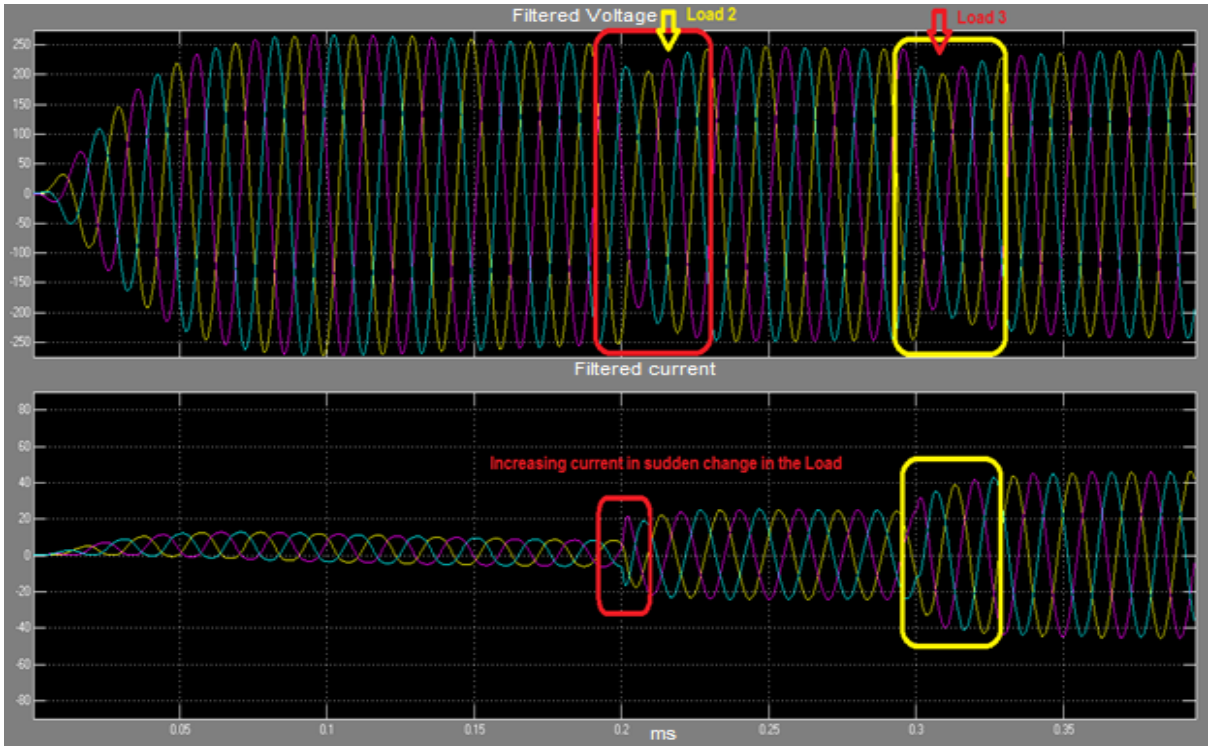


Figure 6.1 Three Loads applied from 0 to 0.4 s

The proposed switched inductor HPB-QZSI is simulated in Matlab/Simulink. The switches in the inverter are turned ON using maximum boost modulation strategy. The output filtered phase voltage and phase current waveforms for three different loads from 0 to 0.4 s can be seen in Figure (6.1):

Load 1 from 0 to 0.2 s, Load 2 from 0.2 s to 0.3 s, Load 3 from 0.3 s to 0.4s.

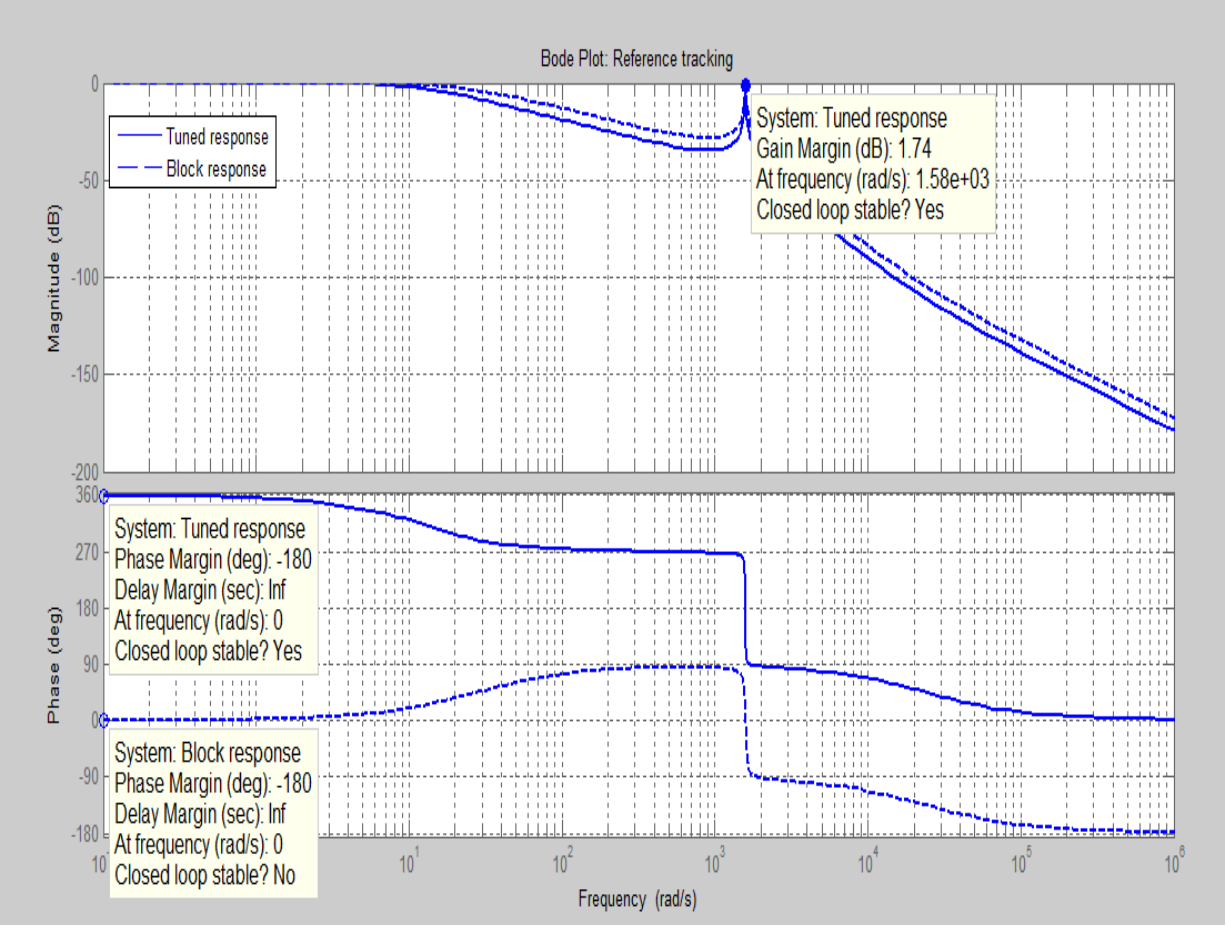


Figure 6.2 Bode Plot: Reference Tracking

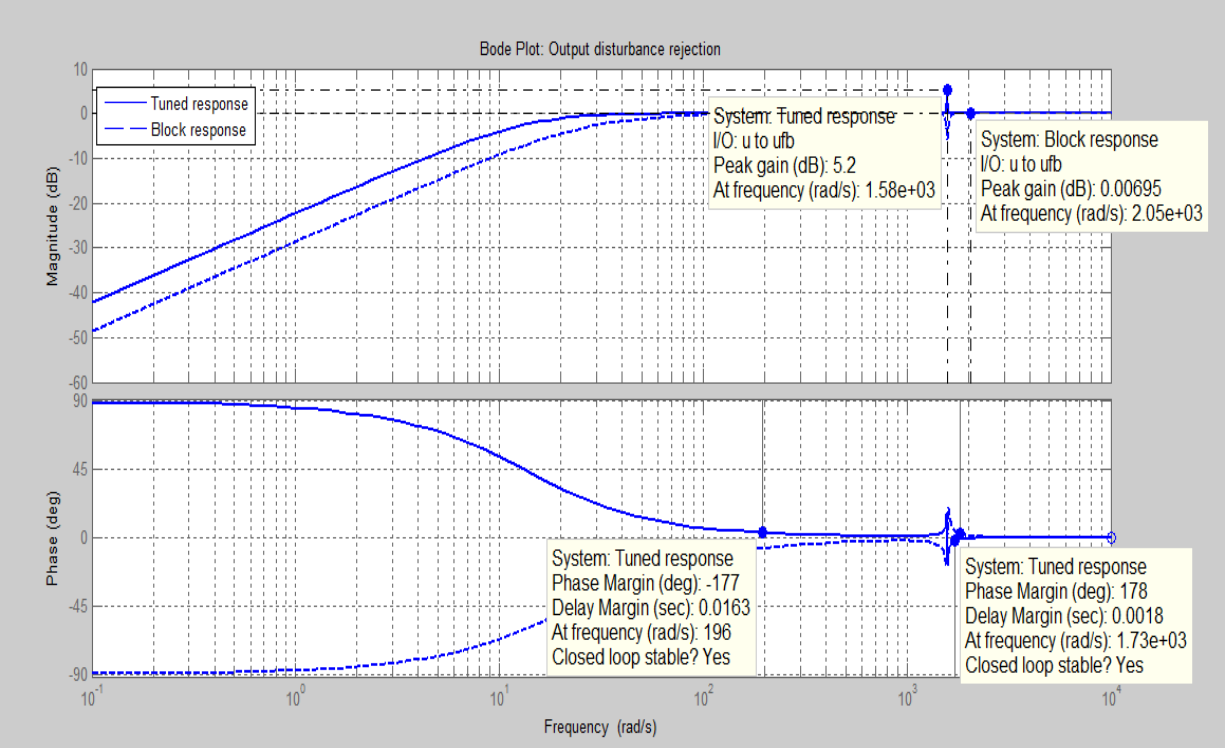


Figure 6.3 Bode plot: Output disturbance rejection

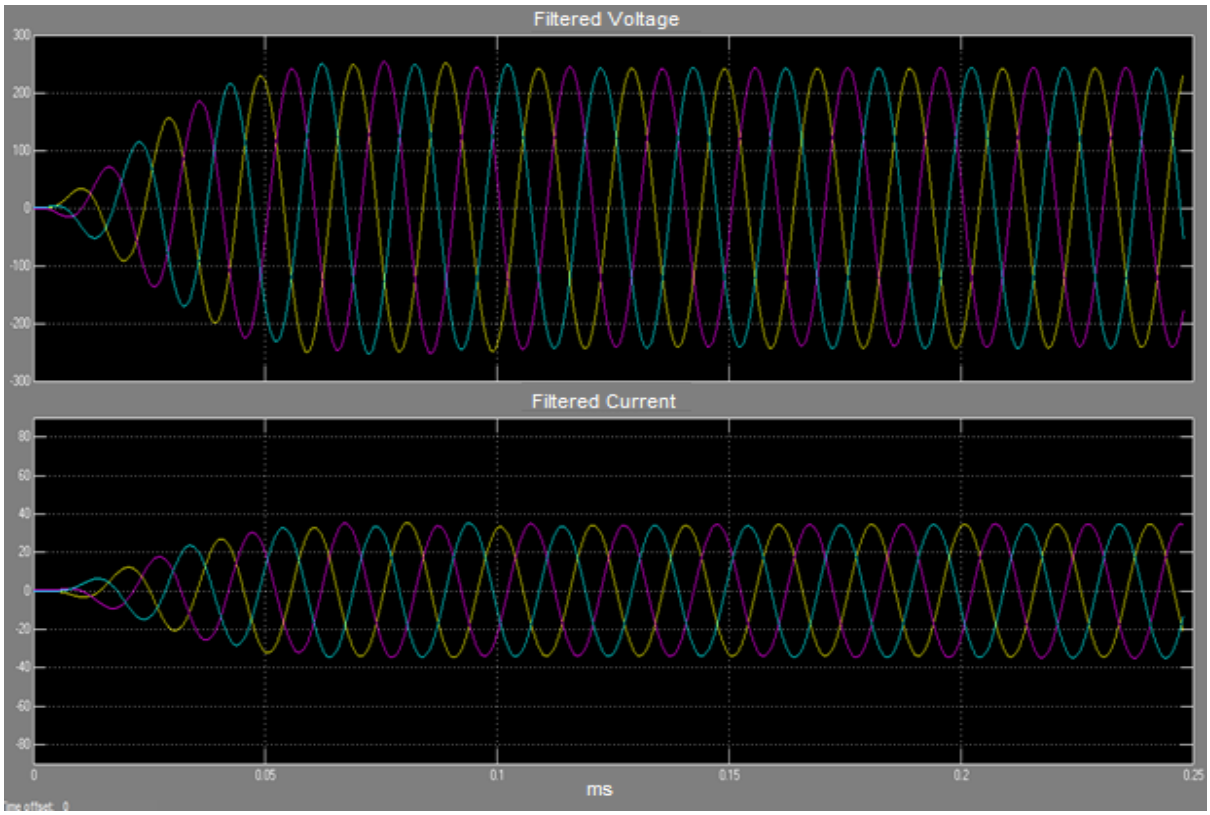


Figure 6.4 the output filtered phase voltage and phase current waveforms for Induction machine of 7.5 kW and 0.3 kVar

The sudden change in load would act as a disturbance to the DC side. From Figures (6.1), (6.2) and (6.3) can be observed that the system has a very good reference tracking and good load disturbance rejection with proposed controller. Figure 6.4 shows the output filtered phase voltage and phase current waveforms for Induction machine of 7.5 kW and 0.3 kVar.

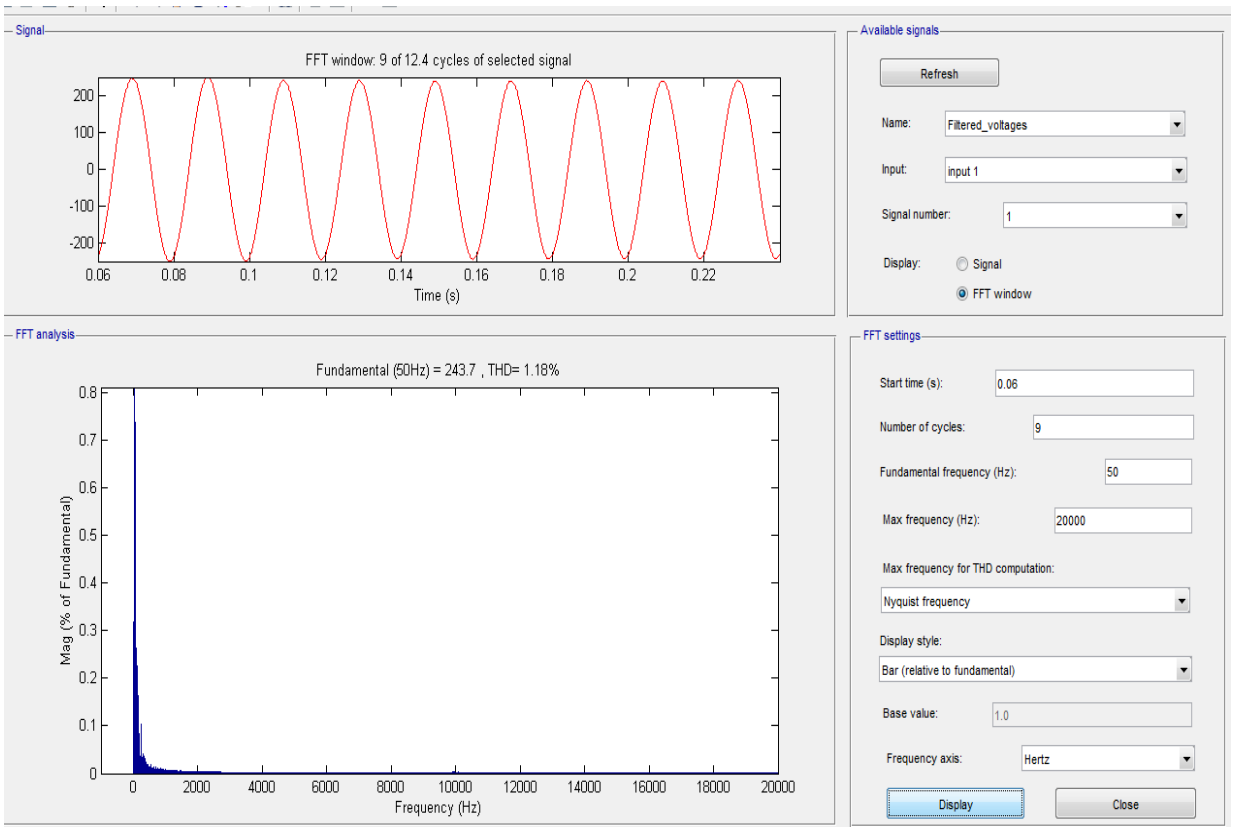


Figure 6.5 FFT analysis- filtered voltage for Induction machine of 7.5 kW and 0.3 kVar

From the simulation results (6.5), it is observed that the fundamental value of filtered phase voltage for induction machine is 243.7 V with THD 1.18 %.

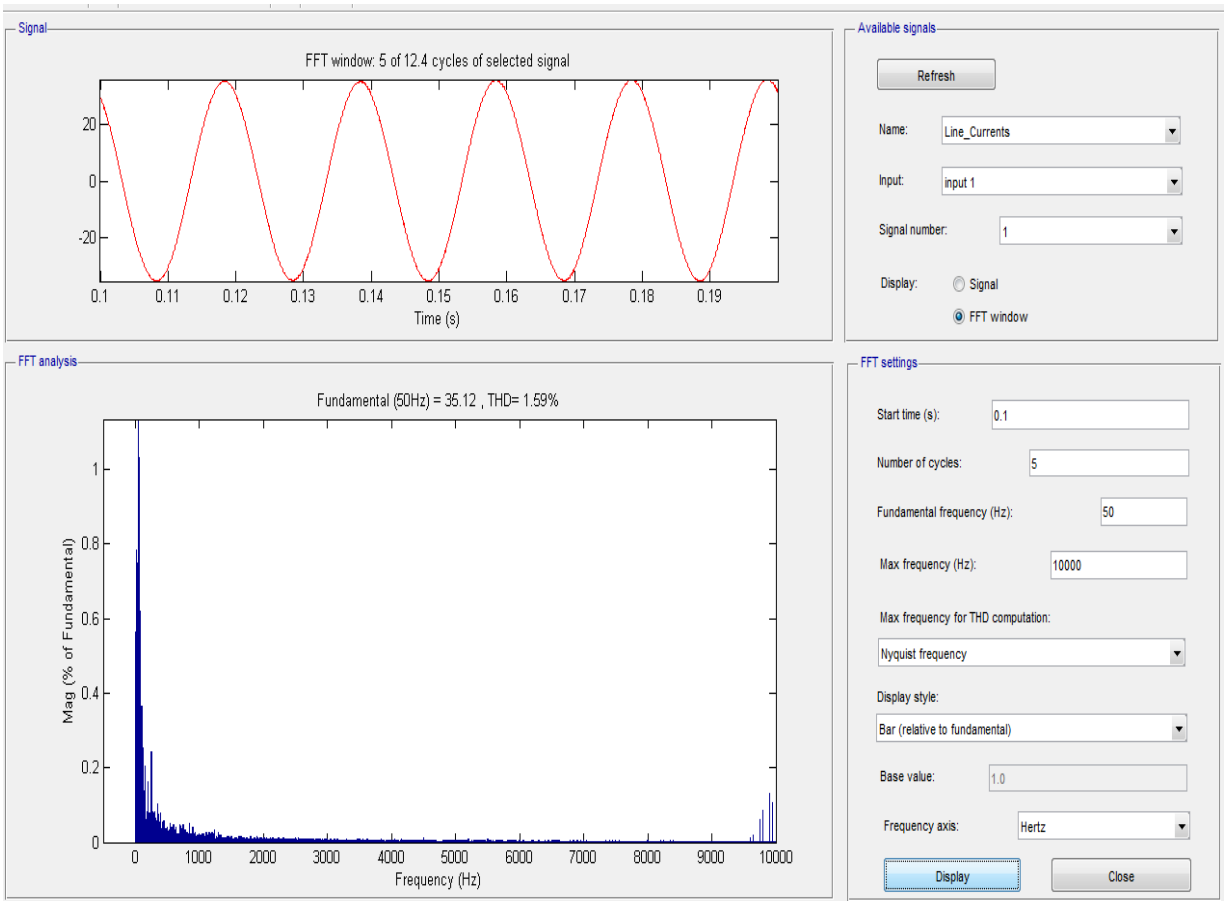


Figure 6.6 FFT analysis - filtered current for Induction machine of 7.5 kW and 0.3 kVar

From the simulation results in Figure (6.6), it is observed that the fundamental value of filtered current for Induction machine of 7.5 kW and 0.3 kVar is 35.12 A with THD 1.59 %.

6.4 Evaluation of the Research Study

The evaluation of this research study is performed by use of Matlab/Simulink simulation and case studies. Based on the form of the simulation results in this thesis, each part can be validated individually with different case studies. Every sub validation is carried out by use of general argument from the simulations results and observation

gained in the different case studies. The result in this research study derived from modelling of the HPB-QZS inverter based on direct control of DC-link voltage, control of AC side, control of shoot-through and active state in Matlab/Simulink.

There is no complete systematic study to reduce the THD and improve the voltage gain due to the complexities and uncertainties involved in the proposed converter control technique. In this section, some of the existing research works are critically reviewed and discussed.

To control the DC-link voltage of the HPB-QZSI, two issues need to be considered. First, the DC-link voltage in the HPB-QZSI is a pulsating value when there is a shoot-through state; thus, it cannot be directly used as a feedback. Second, the small signal analysis of the HPB-QZSI shows that, different from the ZSI (Jingbo et al., 2007) the HPB-QZSI is more vulnerable to the disturbance from the DC input source, especially at higher power ratings, when the ratio between the resistance and the inductance in the system becomes very small. To solve the first issue, (Liu et al., 2011) utilizes the capacitor voltage, inductor current, and the shoot-through duty ratio to estimate and stabilize the DC-link voltage in the QZSI. This approach is also similar to the multi-loop control algorithm of the ZSI presented by (Gajanayake et al., 2007; Ellabban et al., 2012). However, the issue of disturbance rejection from the input voltage is not considered. Although (Xinping et al., 2008b) proposed a disturbance rejection control of the ZSI, the DC-bus voltage cannot be controlled accurately with only a feedforward controller. Also because of the difference in system transfer functions, this method cannot be directly utilized for the QZSI.

The HPB-QZS network has a RHP zero in its control-to-DC peak voltage transfer function, resulting in the DC-link voltages having a non-minimum-phase response. During the non-shoot through states, the DC-link voltage in its peak value V_{DC}, and zero in the shoot-through states. Therefore, the peak DC-link voltage is not suitable to use as a feedback signal. Most of the designer used capacitor voltage as feedback signal, and control the capacitor voltage remains constant. The capacitor voltage V_C is somewhat equivalent to the peak DC-link voltage of inverter, but the peak DC-link voltage is nonlinear to the capacitor voltage. Thus, only controlling the capacitor voltage V_C cannot bring the high performance due to the non-linear property of the DC-link voltage. In (Gajanayake et al., 2006) was proposed a cascade control system, and achieved good dynamic response and disturbance rejection. An extra current loop increases the cost due to the current sensor and a rather complex implementation.

In another case, the feedback control for DC-link voltage of Z-source inverter, which achieves the good reference tracking and disturbance rejection, has widely studied in (Quang-Vinh et al., 2007; Gajanayake et al., 2006). But there still exist many limitations: Because the DC-link voltage is the square waveform due to the shoot-thought states, capacitor voltage V_C is used for control the DC-link voltage (called as indirect DC-link voltage control). V_C can be maintained constant by controlling the shoot-through duty cycle D_O. However, the peak DC-link voltage is changing and becomes uncontrollable while regulating the shoot through duty cycle. The peak DC-link voltage will change when there is a step change in the input voltage though V_C keeps constant. These effects could be transferred into the output side,

which distorts the output voltage, and increases the voltage stress across the switches. The modulation-to-shoot-through duty cycle transfer function $\frac{Do}{V}$, cannot obtain directly, which increases the compensator design difficulty and deteriorate the transient response of DC-link voltage.

6.5 Simulation results summary for HP-BQZSI topology

The PWM carrier frequency Fc is set to be 10KHz, since the shoot-through state is equally distributed into two parts in ON switching cycle, the switching frequency of S7, i.e., fs, is 20KHz. Assuming that the maximum boost with 3rd harmonic injection PWM generation pattern is used, to obtain the maximum AC output voltage under a certain shoot-through duty ratio.

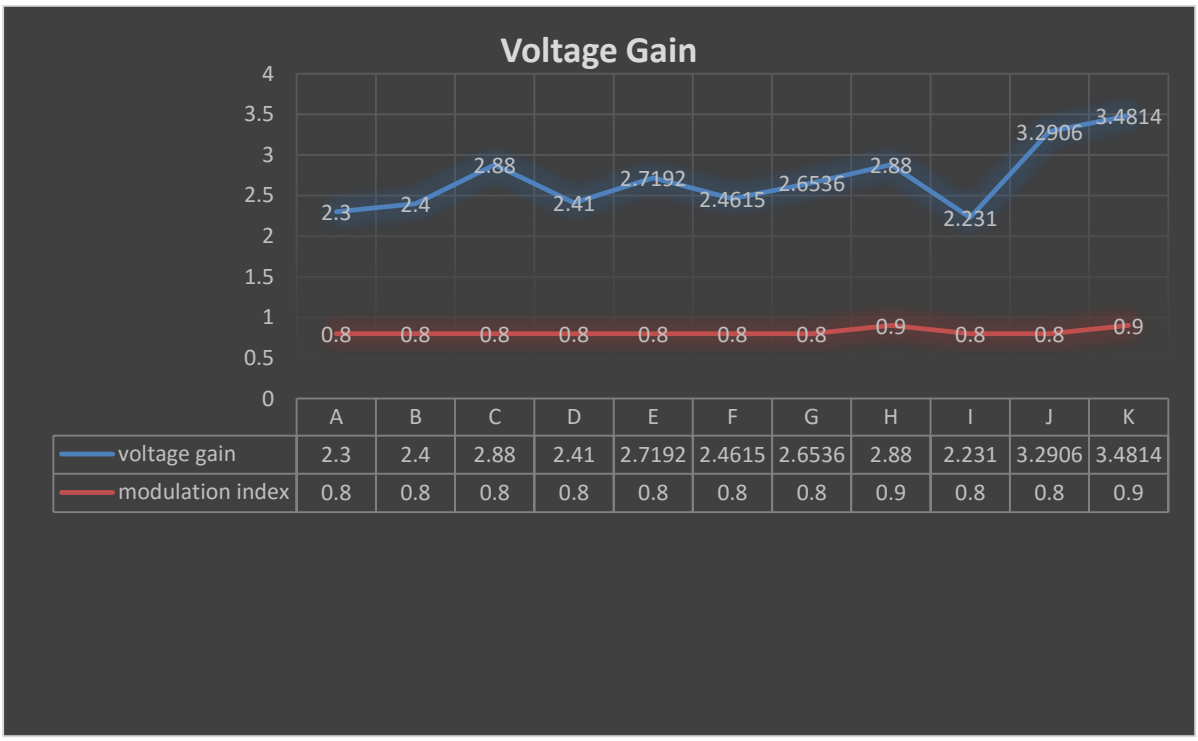
$$V_{ac-rms} = Vin * \frac{(1-D)}{\sqrt{2}(1-2D)} \qquad (6.1)$$

Solving this equation, the maximum shoot-through duty ratio can be calculated as (0.3), therefore, the maximum voltage stress on all switches is

$$Vpn = Vin \frac{1}{1-2Dmax} \qquad (6.2)$$

6.5.1 Comparison between proposed method and other research methods

Comparison between proposed control method and other research methods is shown in figure (6.7) the control technique proposed, offers good output voltage boost properties and relatively simple power circuit. Even so extensive simulations of the proposed techniques are to be performed to verify its ability to ensure necessary output voltage at all defined operation modes. Although, a top down approach was identified as a best available technique for improving the voltage gain [See Figure (6.7)], and reducing harmonic distortion caused by number of branches and loads [See Figure (6.8)]; likewise switching losses also need to be considered by using high frequency modulation ratio.



	A	B	C	D	E	F	G	H	I	J	K
voltage gain	2.3	2.4	2.88	2.41	2.7192	2.4615	2.6536	2.88	2.231	3.2906	3.4814
modulation index	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.9	0.8	0.8	0.9

Figure 6.7 Comparison between proposed method and other research methods

A: SPWM + Z-Source Inverter

B: Double Carrier + Z-Source

C: 3rd harmonic current injection in renewable energy

D: Vector Modulation + Current Fed QZ-Source

E: 3rd Harmonic Injection+ Phase Shifting+ multilevel Inverter

F: 3Level QZS-inverter+ New Boost Modulation Technique

G: quasi-Z-source+ Close loop control method

H: SPWM+ QZ-Source Inverter

I: PWM+ Fuzzy Logic Control+ Z-Source Inverter

J: Double carrier+ QZSI+ Renewable energy

K: Proposed Control Technique

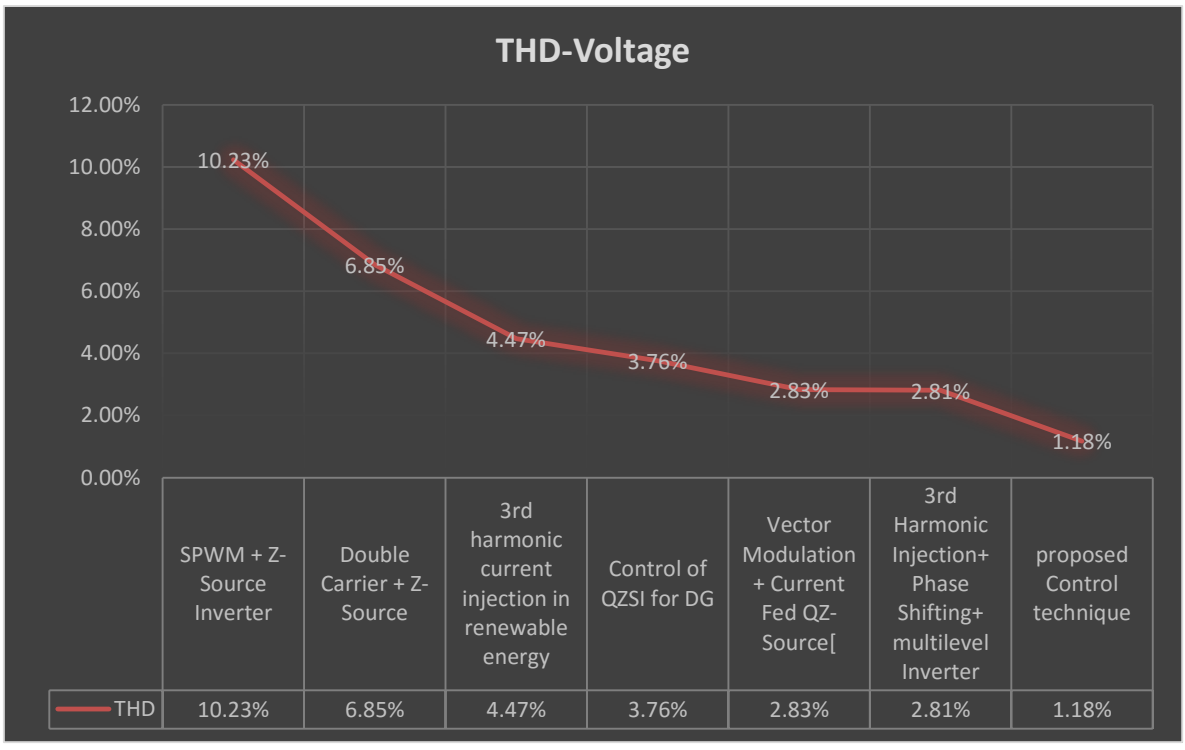


Figure 6.8 Total harmonic distortion

Table (6.1) gives references for the above mentioned data.

Table 6.1 THD's References

(N.Muruganandham, 2013)	(Ali and Kamaraj, 2011b)	(Chandragupta Mauryan, 2013)	(Yuan et al., 2009)	(Qin et al., 2014)	(Colak et al., 2010)
10.23%	6.85%	4.47%	3.76%	2.83%	2.81%

Table 6.2 Percent of the Harmonic Current Distortion

Individual harmonic order h(odd harmonics)	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	THD
IEEE std. 1547	4.0%	2.0%	1.5%	0.6%	0.3%	5.0%
(Yuan et al., 2013)	1.21%	0.58%	0.38	0.28%	0.25%	2.92%
Proposed control method	0.41%	0.27%	0.16%	0.14%	0.07%	1.59%

Table (6.2) gives the individual harmonic order of current distortion in percentage.

Chapter 7

Conclusion and Further work

7.1 Conclusion

This chapter summarizes the key points and important outcomes of the thesis. A close study of all the relevant topologies reveals that the modifications are motivated by one or more of the following reasons:

1) Improve efficiency
2) To increase the voltage gain
3) To reduce the number and size of both active and passive devices
4) To reduce the voltage stress on the active and passive devices
5) Optimal utilization of input voltage to maximize the output voltage

Most of experiments and simulation studies applied to the power systems shows that the conventional controllers have large overshoots and long settling times. Also, optimizing time for control parameters, especially PI controllers, is very long and the parameters are not calculated exactly. In addition, it has been known that conventional controllers generally do not work well for nonlinear, higher order and time- delayed linear, and particularly complex and vague systems that have no precise mathematical models. It is appropriate for rapid applications.

Modified high-performance bidirectional quasi-Z-source can overcome limitations of traditional quasi-Z-source inverter which can operate at wide range load (even no-load) with small inductor, eliminate the possibility of the DC-link voltage drops, and simplify the inductor and controller design. The operation modes, voltage relationship of the new high performance bidirectional quasi-z-source inverter, and control strategy for switch $S7$ has been described in detail. The result shows that there is no distortion on the DC-link voltage v_{PN} and the voltage across the switch $S7$, which indicates that there is no discontinuous current in the inductors and the switch. Therefore, the system is working in the continuous conduction mode (CCM). The input current ripple is directly related to the current ripple in the inductor, and under this maximum voltage test condition, it achieves the designed maximum current ripple. Because of the front capacitor, the ripple current in the inductor is filtered out and a smooth current is obtained at the DC input side.

The modulation of the QZSI is different from the H-bridge inverter because of the shoot through state. The way of adding the shoot-through state influences the quasi-Z-source network design and the system efficiency. Compared with the triangular carrier-based method, the shoot-through period of the modified method is merged into one part.

It is apparent that increasing the switching time and decreasing the switching frequency decreases the total losses but main drawbacks are increasing EMI noise

and reducing quality of power converters due to increasing the ripple on output voltage or current.

In this thesis, direct control methods are reviewed and compared for bidirectional and high performance QZSI under the same input voltage, shoot-through duty ratio, peak DC-link voltage across the inverter, switching frequency and output load. The simulations have been developed in Simulink/Matlab. Three different loads are connected at the output of the HPB-QZSI, namely, Induction machine of 10 kW and 0.3 kVar from 0 to 0.2 s followed by R-L load of 8 kW and 0.30 kVar applied from 0.2 s to 0.3 s, finally, R-L load of 8.5 kW and 0.30 kVar applied from 0.3 s to 0.4 s.

The comparison result shows that the proposed shoot-through insertion PWM control method is the most suitable method for renewable energy sources (RES). It requires less inductor value and results in less switches voltage stress, less total harmonic distortion and higher efficiency.

In the other control methods modulation index has to be minimum to get maximum boost factor. But the voltage stress increases with minimum modulation index. This limitation is eliminated in the newly proposed sawtooth carrier PWM with 3rd harmonic injection in direct control system.

This control method has the following advantages over the other traditional control methods:

- Switching loss is reduced as only one of the phase leg is gated during shoot-through states.

- It involves alternative active state and shoot-through state and no zero states. Hence, it reduces the ripple content in inductor current.
- The voltage stress across the switches is reduced as modulation index could be kept high.
- This method enhances the fundamental voltage by reducing the total harmonic distortion.

The techniques, which used in simulation, are presented to show how they are used to investigate different switching schemes. Incommensurate properties of this network open a new horizon to researchers and engineers to explore, expand, and modify the circuit for a wide range of power conversion applications.

7.2 Future work

Large volume customers of power electronics have driven power electronics development. These markets include motor drives, UPS, electric cars, inverters/converters for solar, micro-turbines, fuel cells, and switching mode regulated AC and DC power supplies. The results of product evolution are benefiting all users; however, there are problems unique to distributed generation that has limited the manufacturers of PV inverters to a few smaller companies. These companies have not had the required sophisticated research and reliability programs or manufacturing methods necessary to develop a mature product Thus, the present approach to PV inverter supply has low probability of meeting Distributed Objects Everywhere (DOE) reliability goals. Several factors lead one to believe that inverter reliability can be

dramatically improved. These include improvements in technology, increasing numbers of product, and constantly improving manufacturing techniques. These will eventually spill over into distributed energy inverters; however, a significant R&D effort could accelerate that process so that the "Inverter for the 21st Century" could be developed.

Areas for future work include:

- Investigate the impact on the DC-link voltage ripple for different switching schemes.
- Investigate the performance in over-modulation operation region.
- For a severely unbalanced load, or nonlinear load, control schemes such as predictive control, or repetitive control are more compatible with the digital controller, therefore develop a model implementing these controllers may achieve good performance.
- A study of the relationship between the neutral current and load condition may produce a better controller design. The neutral current contains information on the load conditions, which may be used for better control design.
- Evaluate the performance of the scheme at a high voltage level more suitable for power system applications.

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Appendix

Appendix 1

Novel Control Technique for Quasi Z-Source with Improved Voltage Gain and reduced THD

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Novel Control Technique for Quasi Z-Source with Improved Voltage Gain and reduced THD

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***Abstract*— A novel control technique for step-up DC/AC renewable energy converter to improve the voltage gain, efficiency and reduce total harmonic distortion (THD) is investigated. The main drawback of the conventional control techniques for DC/AC conversion is drawn from the multistage energy conversion structure which implies complicated control, protection algorithms and reduced reliability due to the increased number of switching devices. To overcome this problem, combination of quasi impedance voltage fed source inverter with a modified double carrier based SPWM in simple operation condition for maximum constant boost control with 3rd harmonic injection is proposed. This is achieved by voltage-fed quasi impedance source inverter with continuous input current implemented at the converter input side and it can boost the input voltage by utilizing extra switching state with the help of shoot-through state technique. The proposed strategy gives a significantly high voltage gain compared to the traditional PWM techniques since all the zero states are converted into shoot-through states.**

Keywords-component;Quasi-Z-source,SPWM,THD,Voltage Gain

Introduction

Among renewable energy sources, the wind and photovoltaic energy is being widely utilized because of their abundance and sustainability to generate electricity. In wind and PV based power conditioning systems, the interface converter system acts as the major key components. Z–source DC/AC converter have been recently proposed for alternative power conversion concept as they have both voltage buck and boost capabilities [4]. These inverters use a unique impedance network coupled between the power source and inverter circuit, to provide both voltage buck and boost properties, which cannot be achieved with conventional voltage source and current source inverters. Z-source inverters are adapted as power conditioning circuits because they combine the functions of voltage boost and DC-AC conversion. The quasi impedance source inverter is a modified topology derived from the Z-source inverter topology, employing an impedance network which couples the source and the inverter to achieve voltage boost and inversion [4].The conventional voltage source inverter (VSI) and current source inverter (CSI) suffer from the limitation that triggering two switches in the same leg or phase leads to short circuit. In addition, the maximum obtainable output voltage cannot exceed the dc input. Both Z-source inverters and quasi-Z-source inverters overcome these drawbacks; by utilizing several shoot-through zero states, in which two switches in the same leg are fired simultaneously to boost the output voltage [3]. Sustaining the six permissible active switching states of a VSI, the zero states can be partially or completely replaced by the shoot through states depending upon the voltage boost requirement [9]. Quasi-Z-source inverters (QZSI) acquire all the advantages of traditional Z-source inverter. It has single stage power conversion, high performance, minimal component count, increased efficiency, improved power factor and reduced cost [2]. The obtained AC voltage must be pure sinusoidal but it can't obtained because the harmonic content are highly present [16]. Higher order harmonics are eliminated by with the help of filters [8]. Here impedance network act as a filter to reduce the lower order harmonics [16].

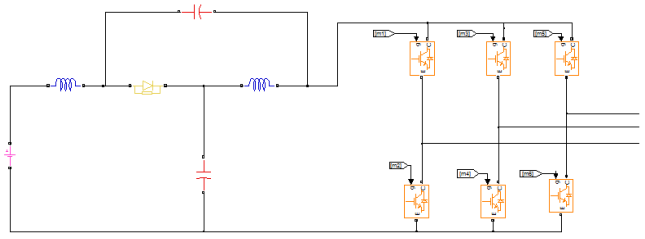

Figure.1 Quasi-Z-Source Inverter

These advantages make the QZSIs suitable for power conditioning in renewable energy systems like wind energy, photovoltaic cells, fuel cells etc. Many carrier based pulse-width modulation (PWM) control methods have been developed and used for QZSIs [16], [15], [11].

Traditional PWM Techniques for QZ-Source Inverter

Generally, traditional inverter has eight permissible states: six active and two zero states. The QZSI has an additional zero state the so-called shoot through state which will be inserted in the switching pattern. In order to an output voltage boost to be obtained, a shoot-through state should always be followed by an active state, i.e., shoot through states should be combined with no influence on the active states. Therefore, minor modifications in the traditional three phase sinusoidal PWM technique will yield various PWM control strategies for the QZSI. The shoot-through zero state does not affect the PWM control of the inverter, because it equivalently produces the same zero voltage to the load terminal. The available shoot-through period is limited by the zero-state period that is determined by the modulation index. There are three available PWM control strategies for QZSI. Traditionally, they are three control methods.

SPWM technique will yield various PWM control strategies for QZSI.

Simple Boost control

Simple boost control uses two straight lines equal to or greater than the peak value of the three phase references to control the shoot through duty ratio in a traditional SPWM. For this simple boost control, the obtainable shoot-through duty ratio decreases with the increase of modulation index. The maximum shoot-through duty ratio of the simple boost control is limited to (1-M), thus reaching zero at a modulation index of one. In order to produce an output voltage that requires a high voltage gain, a small modulation index has to be used. However, small modulation indexes result in greater voltage stress on the devices.

Maximum Boost Control

Maximum boost control turns all traditional zero state into shoot through state. The voltage stress across the switching device is greatly reduced by fully utilizing the zero state. However doing so also cause a shoot through duty ratio varying in a line cycle, which cause inductor current ripple. This will require a high inductance for low frequency or variable frequency application.

Maximum Constant Boost Control

In order to reduce value and cost, it is important always to keep the shoot through rather constant. At the same time a greater voltage boost for any given modulation index is desired to reduce the voltage stress across the switches. This method achieves maximum boost while keeping shoot through duty ratio constant all the time. Also reducing ripple content in inductor current.

Third Harmonic Injection

Third harmonic injection is commonly used in a three-phase inverter system to increase the modulation index range and to increase system voltage gain range. How to choose third harmonic phase, frequency and amplitude to inject?

1. Frequency is 3 times the fundamental (third harmonic): 3ω
2. Phase: must be in phase with reference, so peak cancellation occurs.
3. Amplitude: this can be solved analytically (quite cumbersome algebraic procedure).

Solution is: $V^*_3 = 1/6\ V^*$ (IEEE Std 519)

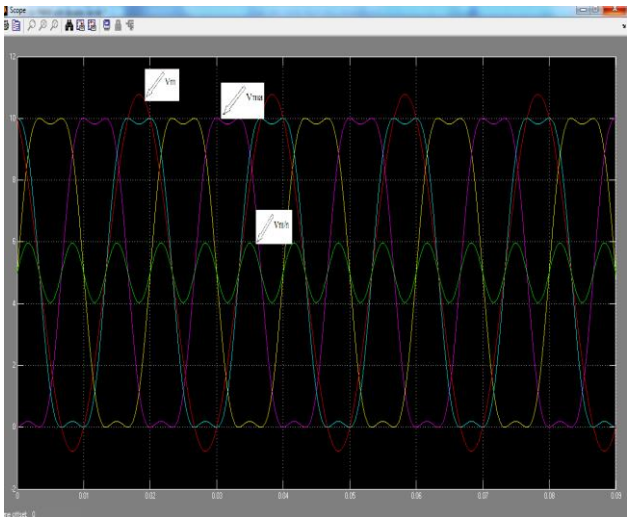

Figure.2 Third Harmonic Injection

Consider the modified references for phase *a* and *b*: [14]

$$V^*_a = V^* \sin(\omega t) + V^*_3 \sin(3\omega t) \quad (2)$$

$$V^*_b = V^* \sin(\omega t - 2\pi/3) + V^*_3 \sin(3(\omega t - 2\pi/3)) \quad (3)$$

After modulation (SPWM) the phase voltages are:

$V_{aN} = V^* \sin(\omega t) + V^*_3 \sin(3\omega t) + V_{hf}$ (4)

$V_{bN} = V^* \sin(\omega t - 2\pi/3) + V^*_3 \sin(3(\omega t - 2\pi/3))$ (IEEE Std 519)

Then the line-line voltage V_{AB} is:

$V_{AB}=V_{aN}-V_{bN}=V^* [\sin(\omega t)-\sin(\omega t-2\pi/3)] + V^*_3[\sin(3\omega t)-\sin(\omega t-2\pi)]$ (6)

$V_{AB}=\sqrt{3}\, V^* \sin(\omega t+\pi/6)$ (7)

3rd harmonic has been eliminated in line-line voltage.

This can also be used here to increase the range of **M** so as to increase system voltage gain range. In this control, the maximum modulation index **M=0.8** can be achieved at (1/6) third harmonic injection .The shoot through duty cycle repeats every **(π/3).** We can also get the voltage gain through studying the behaviour during **((π/6), (π/2))** under this control method. The shoot-through duty ratio in this period is described:

$$\frac{To(\theta)}{T} = \frac{2-(M\sin\theta+\frac{1}{6}M\sin3\theta-\left(M\sin\left(\theta-\frac{2\pi}{3}\right)+\frac{1}{6}M\sin3\theta\right))}{2} \quad (8)$$

From the above calculation, the average shoot-through duty ratio is:

$$\frac{To}{T} = \int_{\pi/6}^{\pi/2} \frac{2-(M\sin\Theta+\frac{1}{6}M\sin3\Theta-\left(M\sin\left(\Theta-\frac{2\pi}{3}\right)+\frac{1}{6}M\sin3\Theta\right))}{2} d\Theta = \frac{2\pi-3\sqrt{M}}{2\pi}$$

Double carrier pulse width modulation control for a quasi-impedance source inverter

First time in [5] used from double carrier pulse width modulation for control a ZSI. As mentioned in [5], [1] this method employs three phase sinusoidal reference signals, Va, Vb and Vc and two triangular waves of high frequency as carrier signals.

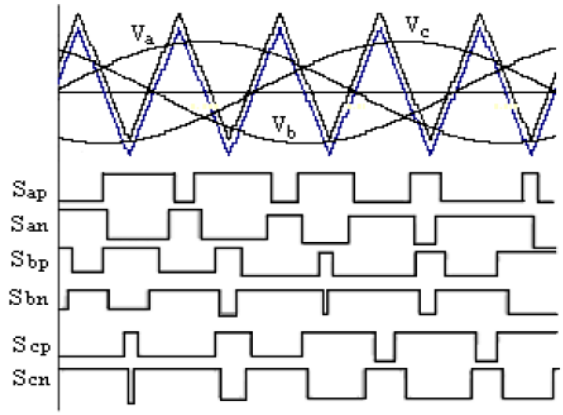

Figure3.Double carrier SPWM

One of the carrier wave is with zero dc offset value whereas the other carrier wave is up-shifted to certain dc offset voltage to control shoot through duty ratio. Gating pulses which are achieved by comparing lower triangular wave (with zero dc offset) and reference wave is given to the upper leg devices of inverter circuit, whereas the pulses obtained by comparing upper triangular wave and reference wave is inverted and given to the lower leg devices of inverter circuit. Fig. 3 shows double carrier control waveforms. In double carrier control method, shoot through duty ratio in varied by varying the dc offset voltage and is derived as:

$Ds=V_{off}/V_t$ (10)

Power total = Power_ACV + Power_DC

Power is proportional to V^2 so

$(V_{rms\_AC}+DC)^2 = (V_{rms\_AC})^2 + (V_{rms\_DC})^2$ (11)

As $V_{rms\_DC} = V_{DC}$ (12)

$V_{rms\_combined}^2 = V_{rms\_AC}^2 + V_{DC}^2$ (13)

Or $V_{DC}^2 = V_{rms\_combined}^2 - V_{rms\_AC}^2$ (14)

So $V_{offset} = V_{DC} = (V_{rms\_combined}^2 - V_{rms\_AC}^2)^{0.5}$ (15)

Unlike other traditional control method such as double carrier unipolar PWM and the double carrier dipolar PWM [11], [12]in double carrier control the duty ratio depends only on the dc offset voltage and hence completely independent of the modulation index.

In this method of the control to get finite voltage gain Ds should be less than 0.5

Relationship of voltage gain versus voltage stress

One important criterion to judge the inverter performance is the relationship of voltage gain versus the voltage stress.

In this condition with the simple operation condition with maximum constant boost control with 3rd harmonic injection.

$V_S = (\sqrt{}3G-1)\ V_O)$ (16)

Voltage Gain = $Vac/(Vs\diagup 2) = ((2Vc - Vo)\ T2 + Vc\ T3)/((T2+T3)Vo)\ M = (2\pi(Vc(1-0.0772M)+0.0386MVo))/(3\sqrt{}3Vo)$ (17)

According to voltage gain we have:

$Vs= (\sqrt{}3G-1)\ V_O= (2.09-0.16M)\ Vc+ (0.08M-1)\ V_O$ (18)

The modulation index M range is from 0.58-1.15. The voltage stress under continuous conduction mode condition can be approximated as VS=2 VC-VO≈ ($\sqrt{}$3G-1) VO (IEEE Std 519)

Novel Proposed Topology

A novel control strategy is combination of double carrier pulse width modulation in simple operation condition for maximum constant boost control with 3rd harmonic injection to step-up DC/AC renewable wind energy converter to improve the voltage gain, efficiency and reduce total harmonic distortion (THD). There are six shoot-through states distributed in a switching cycle, whereas in other traditional PWM techniques only two shoot-through states are inserted in a switching cycle. So in the proposed control technique, the switching frequency viewed from the impedance network is very high; it reduces distortion in the output waveforms.

In the other control method modulation index have to be minimum to get the maximum boost factor but, the voltage stress increases with minimum modulation index. This limitation is eliminated in the double carrier control method since all the zero states are converted into shoot-through states; the high value of voltage gain can also be achieved.

By adding a third harmonic component to the sinusoidal modulating wave, it is possible to increase the fundamental by about 15.5% and, hence, allow a better utilization of the DC voltage. In addition, the reliability of the inverter is greatly improved because the shoot through due to mis-gating can no longer destroy the circuit. Thus it provides a low-cost, reliable, and high efficiency single stage structure for buck and boost power conversion.

Reducing the voltage stress under a desired voltage gain now becomes important to the control of QZ source inverter. As analysed above, the voltage gain is defined as MB, and the voltage stress across the switches is BVdc , therefore, to minimize the voltage stress for any given voltage gain, we have to minimize B and maximize M , with the restriction of that their product is the desired value. On the other hand, we should maximize B for any given modulation index to achieve the maximum voltage gain. Consequently, we have to make the shoot through duty ratio as large as possible.

Simulation Design and comparison

To verify the validity of analysis for the voltage gain of the mentioned control strategies, the QZ-source inverter configuration with the concepts of the control methods have been simulated in Matlab. The purpose of the system is to achieve a maximum boost factor, and compare the voltage gain of the QZ-source inverter under the new control method. Table 1 shows the switching state of QZ-source Inverter. The parameters of the simulated system are as follows: the input dc voltage source is *V*dc=150 V, the QZ-source network inductor and capacitor are *L*1 = *L*2 =1 μ H, *C*1 = *C*2 =1000μ F, The frequency of the triangular carrier signal is taken as 10 kHz to reduce the size of the impedance networks. The inductors in the impedance network limit the current ripple through the devices during boost mode with shoot-through. The capacitors in the impedance network absorb the voltage ripple and maintain a reasonably constant voltage across the bridge. The three-phase *RL* circuit is used as the load of the QZ-source inverter. The voltage stress across the devices (*V*s), the shoot-through duty ratio (*T*0/*T*) and the capacitor voltage of the QZ-source network (*V*C) have been calculated.

The voltage gain of the QZ-source inverter in the maximum boost control method can be calculated as follows:

Voltage Gain: G= (output peak AC voltage)/ (DC link voltage) = 246.8.8/ (150/2) = 3.2906

$V_{link}=\frac{Vs}{2}$ =150/2=75v

Where, V_{link} is the DC link voltage of inverter.

Input voltage Vdc	150 V
Inductors L1, L2	1µH
Capacitors C1, C2	1000µF
Switching frequency	10KHz
L load	10mH
R load	50Ω
Modulation index	0.8
dc offset ratio	%15

Table.1

To investigate this purpose in this paper, simulation was conducted. The simulation results are presented in this section and the relevant waveforms are given. The simulation was carried out with parameters that are shown in table1.

Other properties of simulated system such as type of switches are IGBT/Diode and three-phase RL circuit is used as the load of QZSI.

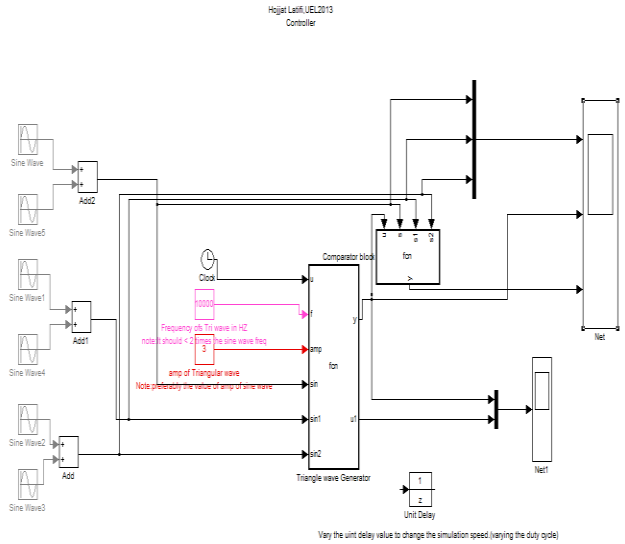

Figure.4 Controller

The triangle wave generator for double carrier program functions is shown in figure 4.

The inverter output voltage is shown in figure.5 is for M=0.8 and maximum boost in Wind energy resources using QZS inverter with variable wind speed (7-12m/s)

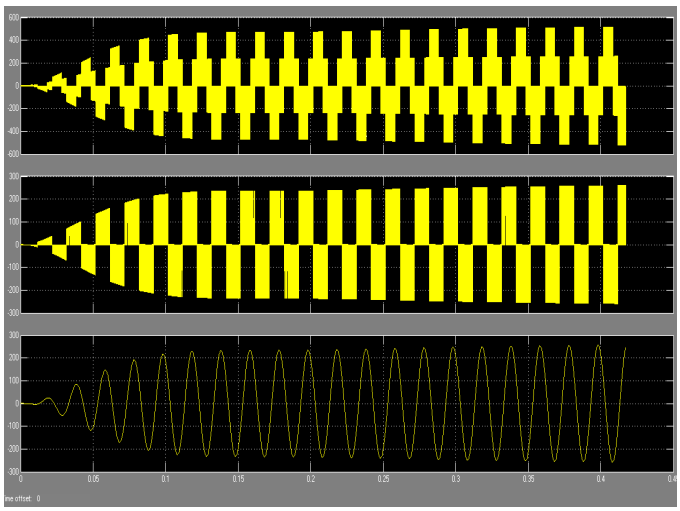

Figure5. Wind system output voltage with the proposed control technique

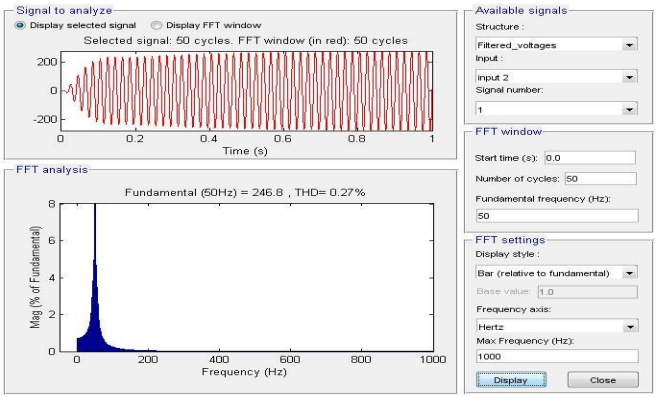

Figure6.The harmonic profile of the load voltage of Wind energy resources using QZS inverter with variable wind speed for double carrier pulse width modulation method.

The harmonic profile of the load voltage of QZSI for double carrier pulse width modulation method is given in Figure.6 which can be seen the amplitude of output line voltage is 246.8V and Total harmonic distortion, (THD=0.27%).

The boost inverter calculation (Duty cycle, Ripple current, Inductor value, Voltage ripple and Capacitor value) is calculated.

Comparison of proposed control techniques with other research methods

Control Techniques	Modulation index	Voltage Gain	THD
SPWM + Z-Source Inverter [10]	0.8	---	10.23%
Double Carrier + Z-Source [5]	0.8	2.4	6.85%
3rd harmonic current injection in renewable energy (K. S. [16]	0.8	---	4.47%
Vector Modulation + Current Fed QZ-Source[7]	0.8	2.41	2.83%
3rd Harmonic Injection+ Phase Shifting+ multilevel Inverter [6]	0.8 1	2.7192	2.81% 2.96%
3Level QZS-inverter+ New Boost Modulation Technique [15]	0.8	2.4615	1.25%
QZ-SI+ Close loop control method[13]	0.8	2.6536	1.186%
SPWM+ QZ-Source Inverter [9]	0.9	2.88	1.16%
PWM+ Fuzzy Logic Control+ Z-Source Inverter [8]	0.8	2.231	0.46%
Proposed Control Technique(Wind System)	0.8	3.2906	0.27%

Benefit of this control method

1. Unlike other method, the boost factor is made independent of the modulation index.
2. Number of shoot through state per cycle of carrier wave increases when compared to other methods.
3. Switching loss is reduced as only one of the phase legs is gated during shoot through states.
4. It involves alternative active state and shoot through state and no zero state. Hence, it reduces the ripple content in inductor current.
5. The voltage stress across the switching is reduced as modulation index could be kept high.
6. This method enhances the fundamental voltage by reducing the total harmonics distortion.

Conclusion

This paper presents a novel control strategy for QZSI utilizing double carrier waveform in maximum constant boost SPWM control with 3rd harmonic injection. This new SPWM gives high boost factor and hence high peak output voltage compared to other triangular carrier based PWM techniques. To compare with other research control techniques [10], [5], [16], [7], [6], [15], [13], [9], [8] this magnitude of lower order harmonics and total harmonic distortion (THD) in the output voltage is found to be reduced. Simulation results presented verifies the analysis of the control method. The QZSI is capable of handling a wide range of input voltage fluctuations. It provides single stage power conversion, features low component rating and cost, and is more reliable. QZSI is best suited interface for renewable energy system and could prove to be highly efficient, when implemented with the improved control techniques proposed.

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