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Performance Analysis and Benchmarking of PLL-Driven Phasor Measurement Units for Renewable Energy Systems

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Abstract: Phasor measurement units (PMUs) are a key part of electrical power systems, providing the dynamic monitoring and control of electrical units and impacting overall operation and synchronization of a network if not properly designed. This paper investigates the use of a phase-locked loop (PLL)-based algorithm for PMUs (to accurately find the magnitude, phase, and frequency) in a three-phase system. Various PLLs are reported in the literature, ranging from the very basic to advanced, capable of dealing with normal and abnormal grid behavior and mainly used for the control of grid-connected converters. In this paper, a number of PLLs were utilized to perform PMU functions, and a benchmarking study has been investigated to analyze the developed PLL-driven PMUs under various grid conditions (such as unbalanced faults, harmonics, and frequency variations). The simulation and experimental results were provided to support the performance capabilities and suggested limitations. In addition, the best PMU in benchmarking was used in the Kundur's two-area system to show the significance of PMUs in a power system.

Keywords: phase-locked loops; phasor measurement units; grid support; control and optimization; grid-connected converters; grid reliability

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1. Introduction

Phasor measurement units (PMUs) are used in power systems to accurately estimate the magnitude, frequency, and phase of the voltage and current's positive sequence components using a common time source [1,2]. However, the increasing integration of renewable energy systems, Direct Current (DC) microgrids, and the excessive use of power electronic converters affect power quality, and thus, PMU performance when estimating the positive sequence phasors is critical to such abnormal grid conditions. Phase-locked loop (PLL) algorithms present an excellent way of estimating PMU quantities and are well-known for their importance and application in grid-connected systems [3]. Consequently, existing systems having PLLs embedded in microcontrollers can be modified and used for performing the extra functionalities of PMUs [4]. The information acquired by PMUs is time stamped with a global positioning system (GPS) and can be transmitted in real time for monitoring and control [4,5]. The input to the PMU is the voltage or current, and the estimated information helps in the monitoring, control, and protection of electrical power systems, improving the overall operation of the entire network [6].

Several phasor estimation algorithms exist in the literature [7–9], such as notch and Kalman filters, Fourier-transform-based methods, level crossing algorithms, and the Shanks method. Simpler methods, where the frequency and amplitude are assumed to be constant, cannot be used for prediction under dynamic grid conditions. Zero-crossing methods [10]

are very easy to implement but presents inaccuracies under harmonics and distorted conditions. The Kalman and notch filtering techniques present undesired filtering delay, which is thus not suitable for PMU applications. The weighted least square method [11] is also used for phasor measurements, but its performance is limited to the real-time speed and computational complexity. The Shanks method discussed in [12] uses an autoregressive moving average (ARMA) model with partial fraction to estimate the phasor vector. However, its performance is limited to the time asymmetry and expansion accuracy of the partial fraction. The short-term Fourier transform (STFT) is a widely used commercial technique but results in measurement errors in case there is a mismatch between the analogue signal and the sampling frequency [13]. A method based on Taylor series expansion and the STFT is suggested in [7], where the estimation accuracy is improved for STFT and the phasor estimation is analyzed under frequency faults. The discrete Fourier transform (DFT) is a well-known method but presents unwanted errors under unbalance grid conditions, and such errors are difficult to remove and may result in the violation of statutory PMU limits [7]. In addition, the DFT presents errors under frequency variations resulting from the picket fence effect and spectral leakage [14]. Many modified DFT methods are proposed in the literature. The authors in [13] improved the accuracy of the DFT under an off-nominal frequency by tracking the frequency of input signals. Likewise, the method discussed in [15] improves the estimation accuracy by adjusting the amplitudes of sample values. These methods, however, require a secondary frequency detector loop, affecting the dynamic response of PMUs. The application of the recursive DFT is suggested in [16] for PMU functionality but suffers from degraded response in the presence of harmonics.

The use of PLLs is very common for the control and synchronization of grid-connected renewable energy systems [17], and thus, it can be extended to be used as a PMU. Very few PLL methods are suggested in the literature for PMU applications. An example of such PLL-driven PMUs is presented in [4,18], where a combination of filters is used and performance has been analyzed under several disturbances. The authors [19] suggested the use of a dual second-order generalized integrator (DSOGI) for estimating the grid voltage phase angle and magnitude under balanced and unbalanced conditions. The method, however, is not fully immune to harmonics (especially close to fundamental) and presents a high-frequency overshoot and an estimation delay. The performance of PLLs is critical in distorted and faulty grid conditions. There exist various advanced PLLs having the capability to deal with unwanted grid conditions such harmonics, DC offset, and unbalanced fault [20–23]. This paper investigates the impact and use of PLLs for estimating the PMU quantities under normal as well as abnormal grid conditions. The PLLs selected for the benchmarking are the synchronous reference frame (SRF)—dqPLL, decoupling network alpha beta PLL (DN$\alpha\beta$PLL) [24], harmonic interharmonic and DC offset (HIHDO) PLL [25], and moving average filter-based enhanced prefiltering ($\alpha\beta$EPMAF)PLL [26]. Thus, in this paper, these PLLs were combined with a post-processing block to discover the phase, magnitude, and frequency of an Alternating Curren (AC) signal. A generic block diagram of a PLL-driven PMU is shown in Figure 1. The voltage or current from the point of common coupling (PCC) or point of connection (POC) in a power system is fed to a PLL. The PLL enables the extraction of amplitude, instantaneous phase, and frequency of the corresponding input quantity. The estimated PLL quantities such as the frequency, voltage/current vectors, and varying phase angle are inputs to the post-processing block to estimate the magnitude, frequency, and phase angle with respect to the synchronous reference (SR). The SR is used to synchronize the PLL instantaneous phase angle with a common time source, i.e., clock signals from a GPS. Note that the outputs of the PLL and the SR are in radians, whereas the output of the PMU (θ_{PMU}^{+1}) is in degrees. The main contribution of this paper involves exploring the use of PLLs for enabling the functionalities of PMUs. Furthermore, PMUs from various existing PLLs and based on analysis and observations were developed by choosing the most suitable candidate to be used in power systems for monitoring and control. The reason for extending PLLs for PMUs is that nearly every grid-connected system employs PLLs, and thus, enabling it to perform an extra function of PMUs would

help in limiting the design complexity and computational burdens on real-time embedded systems.

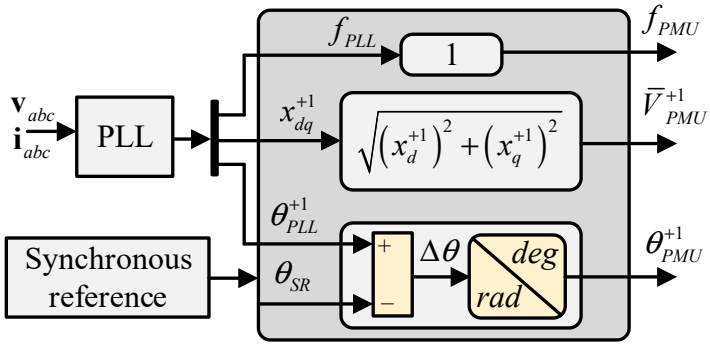

Figure 1. Phase-locked loop (PLL)-driven phasor measurement unit (PMU) model.

The rest of the paper is organized as follows: Section 2 presents the schematic diagram and operating principles for the proposed and benchmarked PLL-driven PMUs. The bode analysis in the actual frequency (Hz) domain is presented in Section 4 to clearly analyze the impact of abnormal grid events on the PMUs transfer characteristics. Section 5 presents the simulation and experimental results for the proposed PLL-driven PMUs. Furthermore, in Section 6, the best PMU in benchmarking was used in the Kundur's two-area power system (having 11 buses and four generators) to show the impact of PMUs on a power system, and fault detection was analyzed.

2. Various PLL-Driven PMUs

This section presents the block diagram, working principle, and features of the four PLLs, which were selected to be used for PMUs.

2.1. SR Frame—qPLL

The dqPLL is suitable for normal grid conditions where a three-phase input signal is transformed to a dq-rotating reference frame with a fundamental angular speed. Subsequently, the q-axis component is passed through a proportional integral (PI) controller and is tracked to zero, finding the frequency and overall input signal angle, as shown in Figure 2. The output of the PI is combined with the nominal grid frequency ω_n, and the estimated PLL frequency ω_{PLL} is calculated followed by an integral. The instantaneous output phase from the PLL is compared to that from the SR, and the phase difference is then calculated. Likewise, the frequency and amplitude are acquired as depicted in Figure 1. The expression for the dqPLL (for the voltage as an input signal) is described as Equation (1), and in general, the three-phase signal is converted to an orthogonal vector $\alpha\beta$ using Equation (2):

$$\mathbf{v}_{dq}^{+1} = \left[T_{dq}^{+1}\right]\left(\underbrace{\left[T_{\alpha\beta}\right]\mathbf{v}_{abc}}_{\mathbf{v}_{\alpha\beta}}\right), \tag{1}$$

$$\left[T_{\alpha\beta}\right] = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \tag{2}$$

where $\mathbf{v}_{abc}$ is the three-phase grid voltage, $\mathbf{v}_{dq}^{+1}$ is the transformed voltage vector in the fundamental SRF frame, $\left[T_{dq}^{+1}\right]$ is the transformation matrix enabling the conversion from $\alpha\beta$ to dq given by Equation (21):

$$\left[T_{dq}^{n}\right] = \begin{bmatrix} \cos(n\theta') & \sin(n\theta') \\ -\sin(n\theta') & \cos(n\theta') \end{bmatrix}, \tag{3}$$

where $\left[T_{dq}^{n}\right]\Big|_{n=+1}$, θ' is the PLL angle.
Subsequently, $\alpha\beta$ is used for control and transformations.

Re-writing Equation (1), the following equations can be obtained:

$$\mathbf{v}_{d}^{+1} = V_m \cos\left(\theta_g - \theta'\right), \tag{4}$$

$$\mathbf{v}_{q}^{+1} = V_m \sin\left(\theta_g - \theta'\right), \tag{5}$$

where V_m is the voltage magnitude, θ_g is the grid angle, and θ' is the estimated PLL angle.

The q-component in Equation (5) results in an instantaneous grid angle when tracked to zero by a PI controller (i.e., $\theta' = \theta_g$).

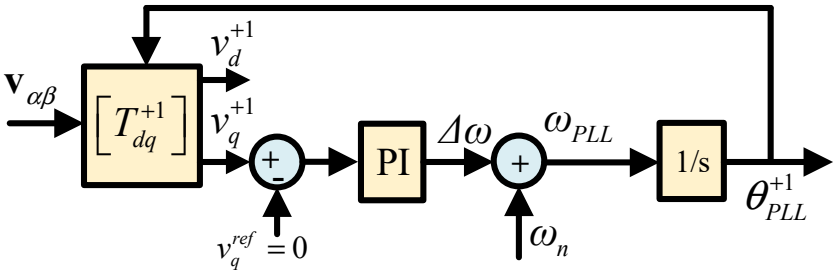

Figure 2. The dqPLL. Note: the input can be a voltage or current.

The dqPLL results in an accurate estimation of the grid angle, frequency, and magnitude under normal grid conditions. However, it fails to estimate these parameters, when the input signal contains asymmetric, DC, and distorted components. This is because the dq-transformation of a signal has more than one frequency component with a specific target speed (n = +1 in this case), resulting in unwanted oscillations on the transformed vector, ascribed by Equation (6):

$$\mathbf{v}_{dq}^{n} = \underbrace{\mathbf{V}_{dq}^{n}}_{DC\ Term} + \underbrace{\sum_{m \neq n} \mathbf{V}_{dq}^{m}\left[T_{dq}^{n-m}\right]}_{Oscillation\ Term}, \tag{6}$$

where $\mathbf{V}_{dq}^{n}$ is a DC term for the sinusoidal signal of the target transformation speed (n = +1) and $\mathbf{V}_{dq}^{m}$ is the magnitude of oscillation for each extra component (m = all other values expect n) present in the input signal. For n = +1, the unbalance, DC, and harmonic components result in double-frequency, fundamental-frequency, and 1-hth-frequency oscillations, respectively.

2.2. DNαβPLL

The DNαβPLL combines multi-sequence decoupling cells developed in the αβ domain for the elimination of selected harmonics and unbalance in the three-phase input signal, so as to extract a clean positive sequence component. The three-phase input signal is transformed into two-equivalent αβ-components $\mathbf{v}_{\alpha\beta}$, and the extraction of various selected components (positive sequence, negative sequence, and harmonics) is enabled using Equation (21):

$$\mathbf{v}_{\alpha\beta}^{*n} = \mathbf{v}_{\alpha\beta} - \sum_{m \neq n}\left[T_{dq}^{-m}\right][F(s)]\left[T_{dq}^{m}\right]\mathbf{v}_{\alpha\beta}^{*m}, \tag{7}$$

where $\mathbf{v}_{\alpha\beta}^{*n}$ is the nth voltage component in the αβ domain, and $[F(s)]$ represents a low-pass filter (LPF) for the removal of residual oscillations, with ω_f being a factor of the nominal grid frequency (i.e., $\omega_f = \omega/4$) and being the cutoff frequency, is expressed as Equation (8):

$$F(s) = \frac{\omega_f}{s + \omega_f}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{8}$$

By using different values of n, desired voltage components are extracted from the actual measured voltage, where m holds all the values other than n. For example, if n = +1, m holds values of −1, +5, −5, +7, and −7. The expression in Equation (21) is repeated for all components, and finally, a combined multi-sequence results in the estimation of n = +1 component, which is important for PMU functionalities. It is worth mentioning that this method in addition to n = +1 also provides the magnitude information of other voltage components (which can be used for converter control).

Finally, once the clean positive sequence component is extracted using Equation (21) with n = +1, the dq-version of the signal is found using Equation (9), which then is useful for control purposes:

$$\mathbf{v}_{dq}^{*n} = \left[T_{dq}^{n}\right]\mathbf{v}_{\alpha\beta}^{*n} = \left[T_{dq}^{n}\right]\left[\mathbf{v}_{\alpha\beta} - \sum_{m\neq n}\left[T_{dq}^{-m}\right][F(s)]\left[T_{dq}^{m}\right]\mathbf{v}_{\alpha\beta}^{*m}\right]. \tag{9}$$

The structure of the DNαβPLL is presented in Figure 3.

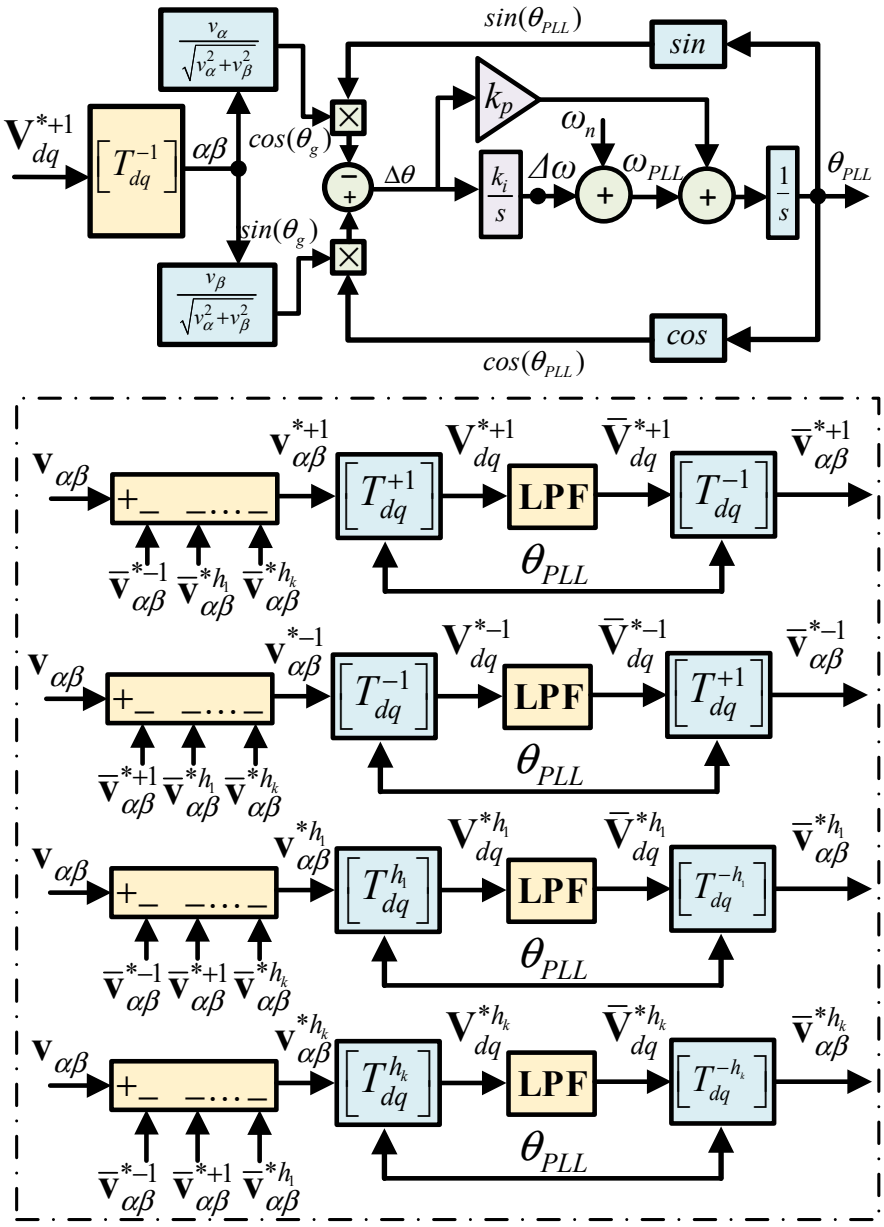

Figure 3. The schematics for the decoupling network alpha beta PLL (DNαβPLL).

The resulting dq-axis positive sequence components are passed through an αβ-PLL to extract the frequency and phase angle. The estimation of the αβ-PLL relies on Equation (10):

$$\begin{gathered}\Delta\theta = \theta_g - \theta_{PLL} \\ \Leftrightarrow \Delta\theta \approx sin(\Delta\theta) \approx sin(\theta_g)cos(\theta_{PLL}) - sin(\theta_{PLL})cos(\theta_g).\end{gathered} \tag{10}$$

The estimation of the αβ-PLL is valid for small errors. The DNαβPLL, however, is resilient to only selected harmonics and is not immune to interharmonics and DC offset. In addition, it presents high complexity among the chosen.

2.3. HIHDO PLL

The DNαβPLL is suitable for cases where the harmonics to be compensated are known and there is no DC offset. However, it fails for unknown harmonic/interharmonic conditions and has a significant number of computations for an embedded microcontroller. The HIHDO employs three decoupling cells for extracting positive sequence components and eliminating DC offset and unbalance. In addition, a harmonic compensation network comprising a high-pass filter (HPF) is used to compensate for the presence of harmonics and interharmonics (not limited to the preselection of the harmonic order). The structure of the HIHDO PLL is depicted in Figure 4. The decoupling cells are employed using the theory of dq-frames, where Equation (6) is rearranged and used to remove the DC (0 Hz) and unbalanced (−50 Hz) components, expressed as Equation (11). The resulting voltage vectors are passed through a configuration of HPFs to effectively compensate the presence of harmonics and interharmonics, given in Equation (12). Equations (11) and (12) are shown as following:

$$\begin{bmatrix} \mathbf{V}_{dq}^{*+1} \\ \mathbf{V}_{dq}^{*-1} \\ \mathbf{V}_{dq}^{*0} \end{bmatrix} = \left[\begin{bmatrix} \mathbf{v}_{dq}^{+1} \\ \mathbf{v}_{dq}^{-1} \\ \mathbf{v}_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(0)} \\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(0)} \\ T_{dq}^{0-(+1)} & T_{dq}^{0-(-1)} & [0] \end{bmatrix} \begin{bmatrix} \overline{\mathbf{V}}_{dq}^{*+1} \\ \overline{\mathbf{V}}_{dq}^{*-1} \\ \overline{\mathbf{V}}_{dq}^{*0} \end{bmatrix} \right], \tag{11}$$

$$\mathbf{V}_{dq}^{+1\prime} = \mathbf{V}_{dq}^{*+1} - \left[T_{dq}^{-1} \right] \frac{\omega_{lf}}{s + \omega_{lf}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \mathbf{V}_{dq}^{*+1}, \tag{12}$$

where $\mathbf{V}_{dq}^{*+1}$ is of interest and is compensated for both the DC offset and unbalance; $\mathbf{V}_{dq}^{+1\prime}$ is the output of the harmonic compensator; ω_{lf} is the cutoff for the LPF. The optimal values of ω_{lf} are $\omega/\sqrt{2}$ for +1 and −1 cells and $\omega/4.5$ for the DC offset compensation cell The $\overline{\mathbf{V}}_{dq}^{*+1}$-filtered version of the compensated dq-vector is found using Equation (13) necessary for subtraction:

$$\overline{\mathbf{V}}_{dq}^{*+1} = \underbrace{\frac{s}{s + \omega_h} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}_{H(s)} \mathbf{V}_{dq}^{*+1}. \tag{13}$$

The value of ω_h ranges from $2\pi 10 \leq \omega_{cH} \leq 2\pi 22$ ($2\pi 50$ nominal frequency) for the optimal performance and dynamics.

The resulting clean positive sequence $\mathbf{V}_{dq}^{+1\prime}$ obtained from the HIHDO is passed through the dq-PLL, and the estimation of the frequency and instantaneous phase angle is enabled. These estimated PLL quantities are later combined with PMU postprocessing to extract the phase, frequency, and amplitude of the input voltage (or current).

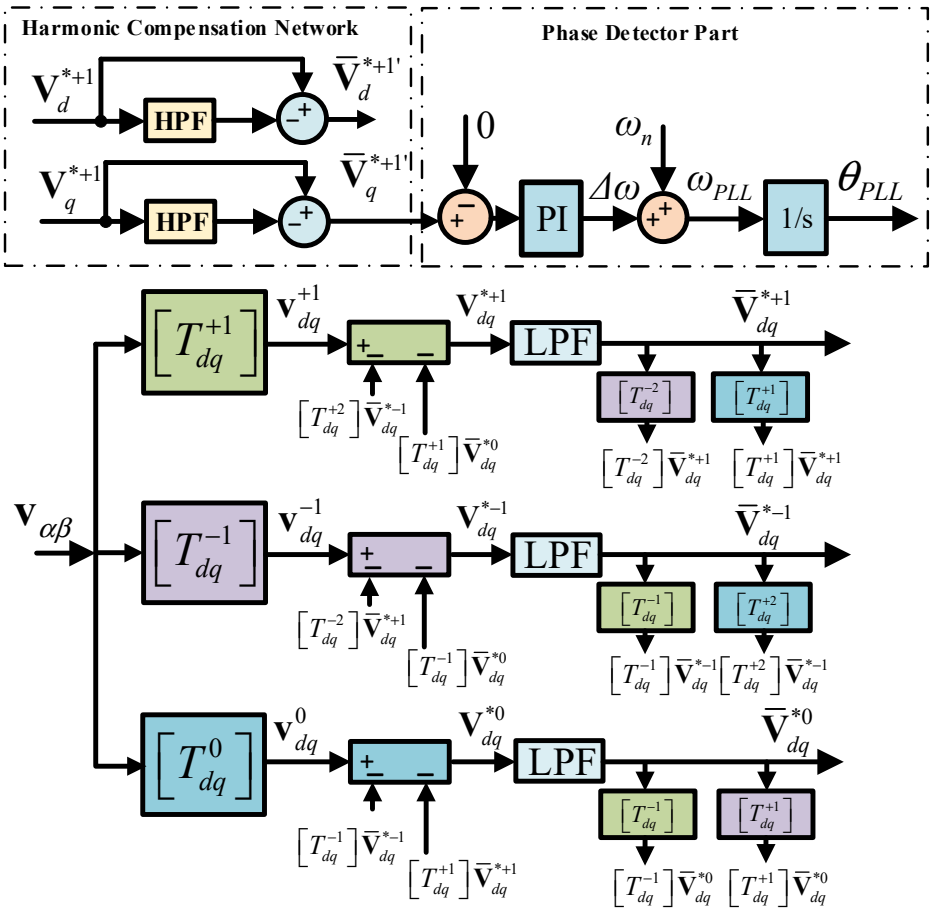

Figure 4. The schematic of the harmonic interharmonic and DC offset (HIHDO) PLL.

2.4. αβEPMAFPLL

A moving average filter (MAF)-based extraction of the phase and the frequency offers saving on computational complexity (requiring one addition, subtraction, and multiplication) and is renowned for its immunity to grid harmonics. The *s*- and *z*-domain transfer functions for the MAF are given in Equations (14) and (15):

$$MAF(s) = \frac{1 - e^{-T_\omega s}}{T_\omega s}, \tag{14}$$

$$MAF(z) = \frac{1}{N}\left(\frac{1 - z^{-N}}{1 - z^{-1}}\right), \tag{15}$$

where T_ω is the window length and is described as $T_\omega = NT_s$ where T_s is the sampling time and N is the number of samples.

The magnitude and phase response of the MAF can be expressed as in Equation (16) using the transfer function of Equation (16):

$$MAF\left(e^{j\omega T_s}\right) = \left|\frac{sin(\omega NT_s/2)}{Nsin(\omega T_s/2)}\right| \angle -0.5\omega(N-1)T_s, \tag{16}$$

where T_s is the sampling time.

However, conventional in-loop MAF techniques suffer from offset error under off-nominal frequencies conditions and low dynamic response due to inherent MAF characteristics posing upper limits on the maximum settling time that can be achieved. Various attempts have been made to improve the dynamic response and estimation accuracy of MAF-based techniques. The main concept in all these techniques is to move the MAF

out of the estimation loop improving the dynamics and add compensation factors for phase drifts. The αβEPMAFPLL uses the MAF in the prefiltering stage (for compensating input harmonics, unbalance, and DC offset) followed by an αβ-PLL. The structure of the αβEPMAFPLL is presented in Figure 5. The input αβ converted from abc is processed by dq-transformation using the nominal frequency ($\omega_n = 2\pi 50$) and is passed though the MAF for filtering and preprocessing. The output of the MAF is retransformed to αβ followed by an αβ-PLL. The MAF, however, offers the phase drift equivalent to Equation (17) under off-nominal frequencies (i.e., $\omega_g \neq \omega_n$), which is shown as following:

$$\angle MAF\left(e^{j\Delta\omega T_s}\right) = -\Delta\omega \underbrace{0.5(T_\omega - T_s)/2}_{k_\varphi}, \tag{17}$$

where $\Delta\omega = \omega_g - \omega_n$. For the compensation of the DC offset, T_ω must be 0.02. This offset error is compensated by adding the compensation factor to the estimated angle of the simple αβ-PLL, as shown in Figure 5. This PLL requires simpler implementation but still presents slightly slower dynamic response.

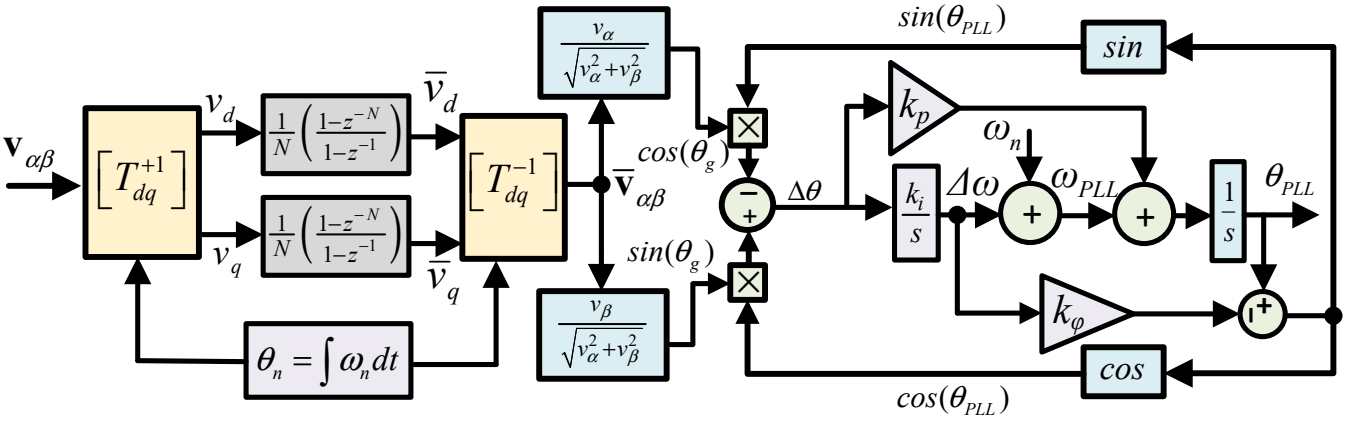

Figure 5. The schematic for the alpha beta enhanced prefiltering moving average PLL (αβEPMAFPLL).

All the PLLs discussed are combined with a postprocessing block (shown in Figure 1), and PMU functionalities are achieved.

3. Frequency Domain Analysis

The PMU performance is critical to the distortion and unwanted frequency components in the input signal (voltage or current), and hence, it is important to analyze the compensation capabilities of PMUs. This requires transfer characteristics and a bode representation where the input is the actual voltage or current signal in the αβ domain and the output is the processed αβ. The conventional dq-PLL is not immune to distortion and DC offset and hence passes all frequencies (no prefiltering). The transfer function for the DNαβPLL is given in Equation (18):

$$\frac{\mathbf{v}_{\alpha\beta}^{*+1}}{\mathbf{v}_{\alpha\beta}} = \left\{ \frac{1 - \left[TFT^{-1} + TFT^{h_1} + \cdots + TFT^{h_k}\right]}{1 - \left[TFT^{-1} + TFT^{h_1} + \cdots + TFT^{h_k}\right] TFT^{+1}} \right\}, \tag{18}$$

where the TFT is the reverse and forward transformation containing an LPF, expressed in Laplace's Equation (19) using the Euler formulation with ω_{fi} as the cutoff frequency of the LPF:

$$TFT^i = \left[T_{dq}^{-i}\right][F(s)]\left[T_{dq}^{+i}\right] = \frac{\omega_{fi}}{s + \left(\omega_{fi} - j \cdot i \cdot \omega\right)}. \tag{19}$$

Likewise, the transfer function for the HIHDO PLL is presented as Equation (20), which contains a combination of decoupling cells and a harmonic network:

$$\frac{\mathbf{v}_{\alpha\beta}^{*+1\prime}}{\mathbf{v}_{\alpha\beta}} = \left\{ \frac{1 - \left[TFT^{-1} + TFT^{0}\right]}{1 - \left[TTFT^{-1} + TFT^{0}\right]TLT_{+1}} \right\} \cdot \left\{ \underbrace{1 - \left[T_{dq}^{-1}\right][H(s)]\left[T_{dq}^{+1}\right]}_{TFT^{+1}} \right\}. \tag{20}$$

Lastly, the transfer function for MAF preprocessing is a combination of an MAF with a forward and reverse transformation and is expressed as Equation (21):

$$\frac{\overline{\mathbf{v}}_{\alpha\beta}}{\mathbf{v}_{\alpha\beta}} = \frac{1 - e^{-T_\omega s}}{T_\omega s}\Big|_{s=s-j\omega_n} = \frac{1 - e^{-T_\omega (s-j\omega_n)}}{T_\omega (s - j\omega_n)}. \tag{21}$$

The transfer functions are depicted in Figure 6, where the DNαβ enables the compensation of the selected low-order harmonics and the HIHDO PLL presents better harmonic and interharmonic compensation with high shifts and negative gains and is independent of the preselection of the harmonic order.

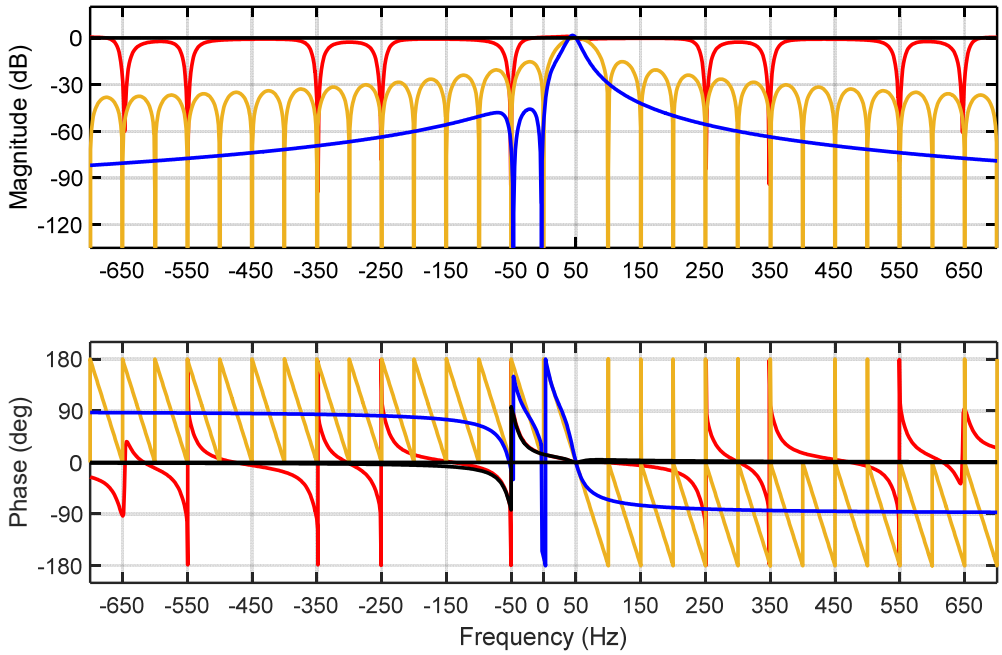

Figure 6. Bode analysis in the prefiltering stage: dqPLL (black), DNαβPLL (red), HIHDO PLL (blue), and αβEPMAFPLL (yellow).

4. Result and Discussion

This section presents the simulation and experimental results.

4.1. Simulation Results

The performances of four PMU algorithms were analyzed under various grid conditions such as harmonic, interharmonics, DC offset, unbalance fault, and phase jump.

The first case (Figure 7) analyzed the response of various PLL-based PMUs to a +30° phase jump (at t = 0.5 s) followed by an unbalanced fault (at t = 0.6 s). The voltage began with normal grid conditions and was subsequently affected by grid faults. The HIHDO PLL presented the best response with faster dynamics among the benchmarks for estimating the frequency and phase angle, whereas it suffered from a slight delay in estimating the magnitude. The voltage magnitude was better estimated by the αβEPMAFPLL; however, a slower response was observed in the frequency and phase angle estimation. The dqPMU,

as expected, suffered from double-frequency oscillations, and the DNαβPMU suffered from high overshoots and slow dynamics.

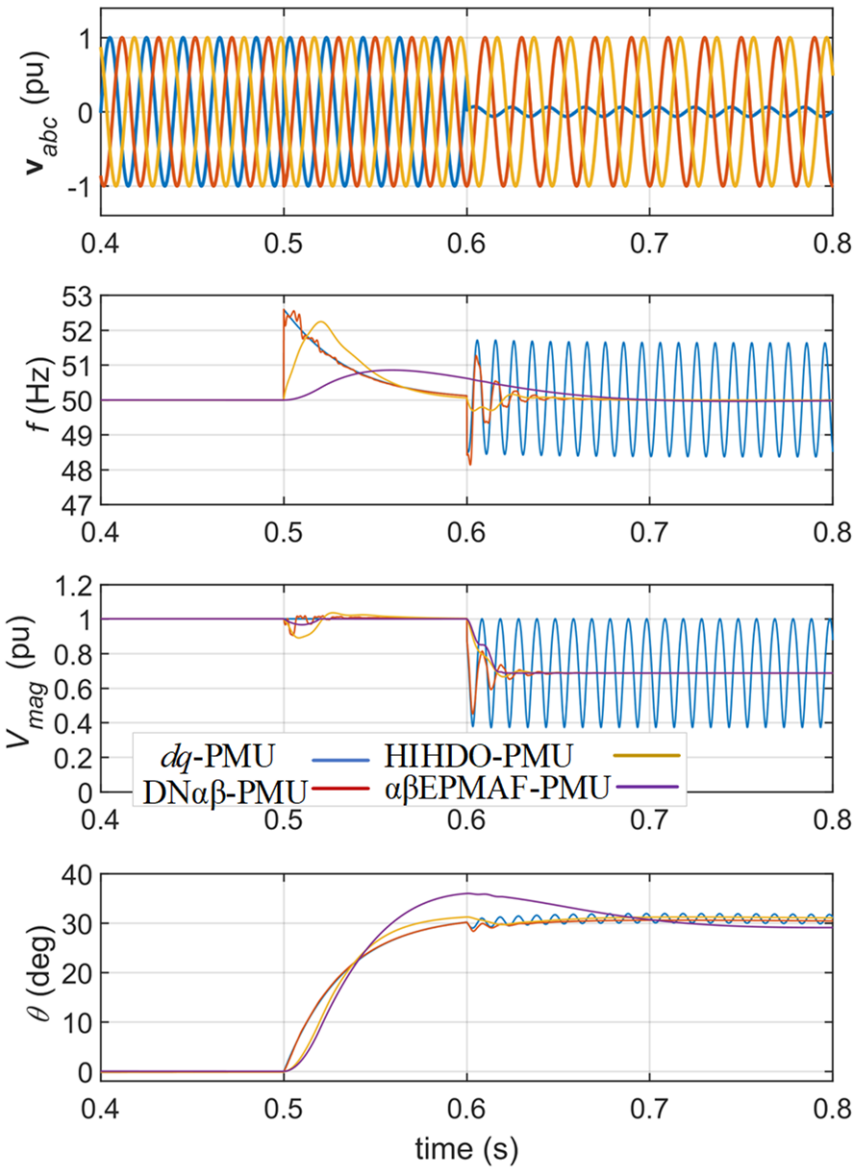

Figure 7. Performance comparison of various PLL-based PMUs under phase fault and sag.

The second case (Figure 8) analyzed the behaviors of the PMUs under a phase jump of −30° (at t = 0.5 s) and harmonic (5% 7th) and DC offset conditions (6%) at t = 0.7 s. The αβEPMAF-PMU, like the first case, lacked a dynamic response with a high settling time for both the frequency and phase angle. The DNαβPMU suffered from high estimation overshoots in the frequency and voltage magnitude. The HIHDO-PMU presented a lower overshoot with a dynamic response similar to that of the DNαβ-PMU for frequency and magnitude responses. These two cases demonstrated the capability of PLLs to mimic the features and capabilities of a PMU, with the HIHDO-PMU presenting the most suitable and desired performance among the benchmarked. The results presented in Figures 7 and 8 are tabulated and summarized in Table 1.

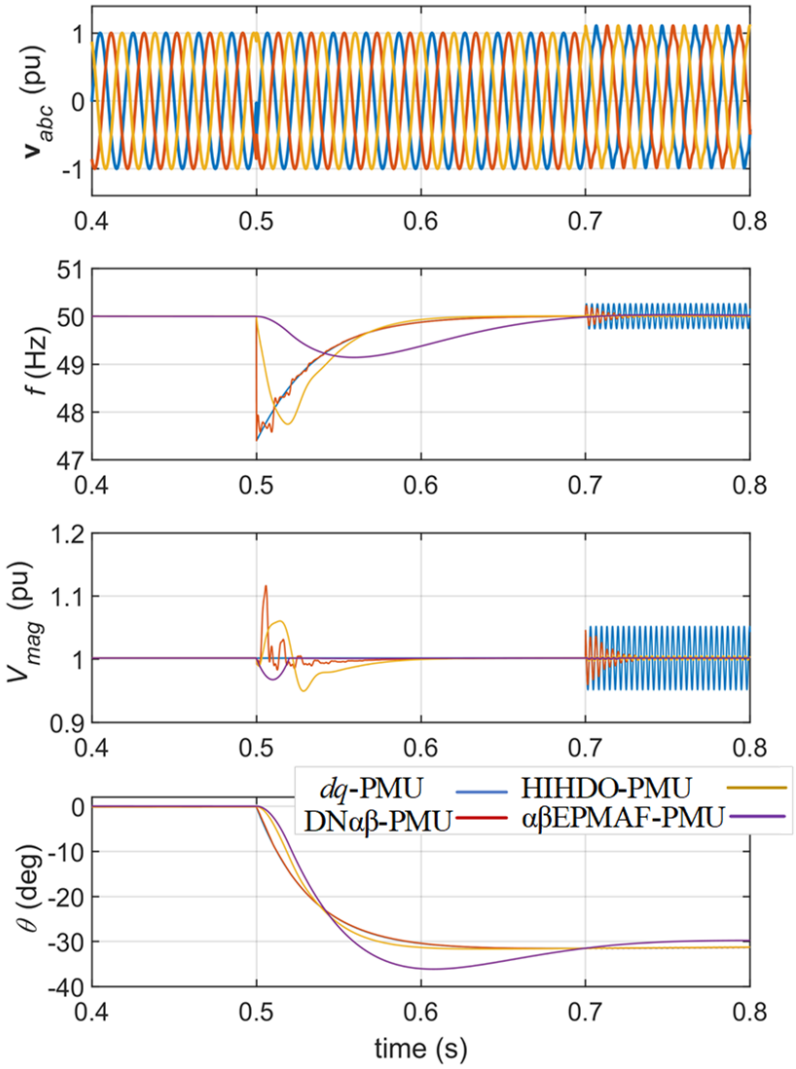

Figure 8. Performance comparison of various PLL-based PMUs under phase fault and sag.

Table 1. Summary of the results presented in Figures 7 and 8.

				Figure 7		Figure 8	
		Fault Types		**Phase Jump**	**Phase Jump + Sag**	**Phase Jump**	**H + DC Offset**
PLL's types	dq-PMU	Overshoot	Frequency (Hz)	2.59	1.71	2.594	0.26
			Voltage magnitude (p.u.)	0	0.628	0	0.051
			θ_{error} (deg)	0	1.851	1.43	0
		Settling time	Frequency (ms)	**	*	132	*
			Voltage magnitude (ms)	0	*	0	*
			θ_{error} (ms)	91	*	0	0
	DNαβ-PMU	Overshoot	Frequency (Hz)	2.59	1.858	2.597	0.227
			Voltage magnitude (p.u.)	0.095	0.23	0.1164	0.0455
			θ_{error} (deg)	0.175	1.635	1.44	0
		Settling time	Frequency (ms)	**	65	128	44
			Voltage magnitude (ms)	43	58	55	59.5
			θ_{error} (ms)	95	36	0	0

Table 1. *Cont.*

			Figure 7		Figure 8	
HIHDO-PMU	Overshoot	Frequency (Hz)	2.24	0.29	2.25	0.0345
		Voltage magnitude (p.u.)	0.108	0.021	0.0604	0.0052
		θ_{error} (deg)	1.24	1.22	1.54	0
	Settling time	Frequency (ms)	**	54	110	*
		Voltage magnitude (ms)	69	41	92	*
		θ_{error} (ms)	**	50	0	0
αβEPMAF-PMU	Overshoot	Frequency (Hz)	0.8572	0	0.857	0
		Voltage magnitude (p.u.)	0.054	0	0.0323	0.0026
		θ_{error} (deg)	5.93	5.86	6.102	0
	Settling time	Frequency (ms)	**	76	196	0
		Voltage magnitude (ms)	21	25.1	20	23
		θ_{error} (ms)	**	135	**	0

Note: * means recurrent oscillations. ** means previous fault does not get settled until next fault. per unit (p.u.).

4.2. Experimental Results

The HIHDO-PMU was further validated in real time experimentally using a Speedgoat® performance real-time target machine and a TELEDYNE LeCroy oscilloscope, shown in Figure 9. The PMU algorithms were developed in MATLAB and loaded to Speedgoat via an Ethernet link, and the outputs were obtained from an IO131 terminal board. Various test cases were considered, such as positive and negative phase changes, voltage sags, and harmonic, interharmonic, and DC-offseted grid voltages, and the real-time operation of the HIHDO-PMU was validated.

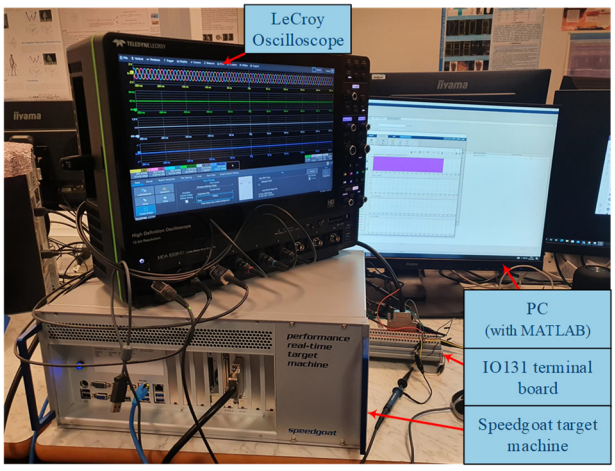

Figure 9. The laboratory experimental setup.

The first experiment analyzed the response of the HIHDO-PMU to a phase fault of +30°. With a zero initial phase angle, a +30° step change was induced in the grid voltage (at the point marked), and its impact on the estimation capabilities was recorded in Figure 10. The PMU responded to this variation in the phase and attempted to track the new reference, where in this process the frequency and voltage estimations experienced small overshoots but were settled quickly with a settling time of 80 ms. The frequency of the overshoot was 2.1 Hz, and the deviation of the voltage magnitude at the point of fault was 0.1 per unit (p.u.). The PMU tracked the phase difference and reached 30° in 70 ms. The result showed that the PMU is robust to the variation in the phase angle and tracks this variation with fast dynamics.

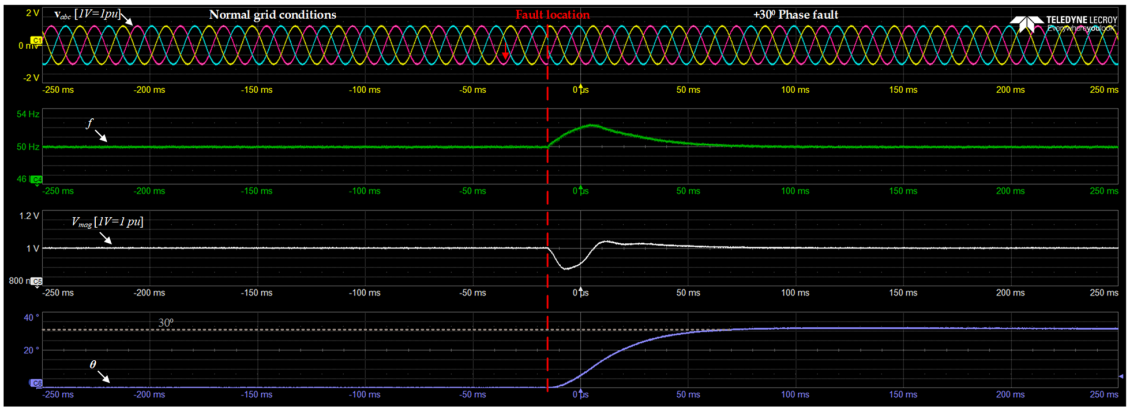

Figure 10. Experimental results for the real-time validation of the HIHDO-PMU under phase fault.

The second case validated the accurate estimation of the HIHDO-PMU under harmonic distortion (Figure 11). The input to the PLL was distorted with 6% 5th and 5% 7th harmonics, and a phase fault of $-20°$ was also introduced. The PMU suppressed the presence of harmonics and resulted in the clean tracking of the amplitude, frequency, and phase angles. The overshot experienced under a phase fault was 1.6 Hz and 0.05 p.u. for the frequency and phase, respectively. The settling times for the frequency, magnitude and phase estimations were 80 ms, 66 ms, and 65 ms, respectively. In the third case (Figure 12), the interharmonic and DC offset compensation of the PMU were validated, demonstrating its suitability for conditions where the input has such components.

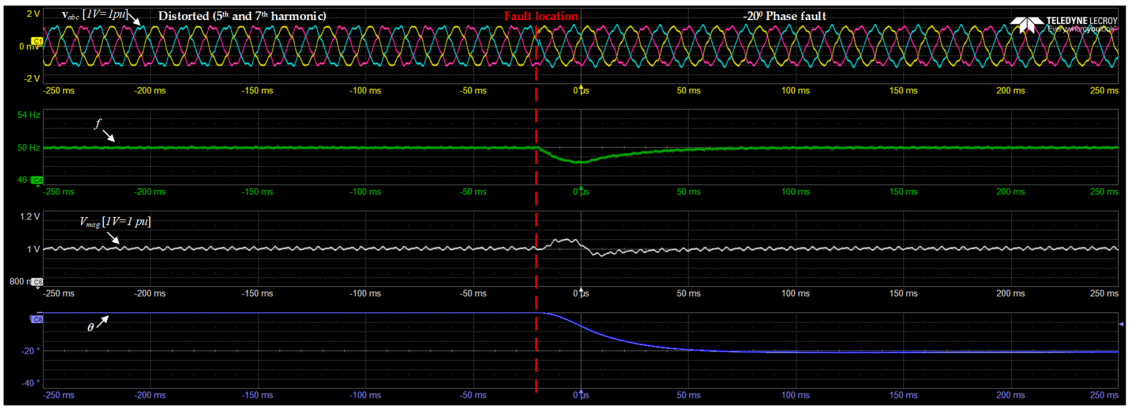

Figure 11. Experimental results for the real-time validation of the HIHDO-PMU under harmonic distortion and phase fault.

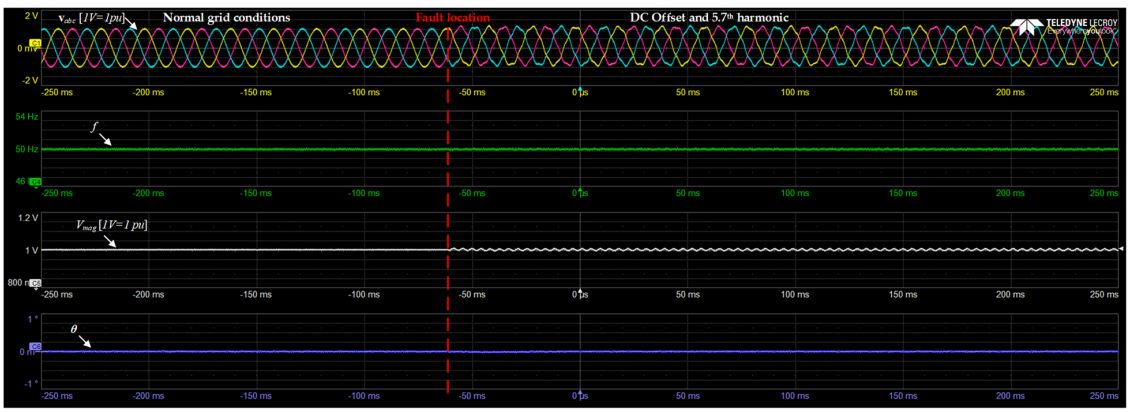

Figure 12. Experimental results for the real-time validation of the HIHDO-PMU under inter-harmonic distortion and DC offset.

The fourth case (Figure 13) combined various faults to verify the robustness of the PMU, i.e., the input to PMU was distorted with 5th and 7th harmonics, followed by a −20° phase fault and a voltage sag of 37%. The PMU enabled the suppression of harmonics, managed the phase change and voltage sag and resulted in the accurate estimation of the frequency, phase angle, and magnitude.

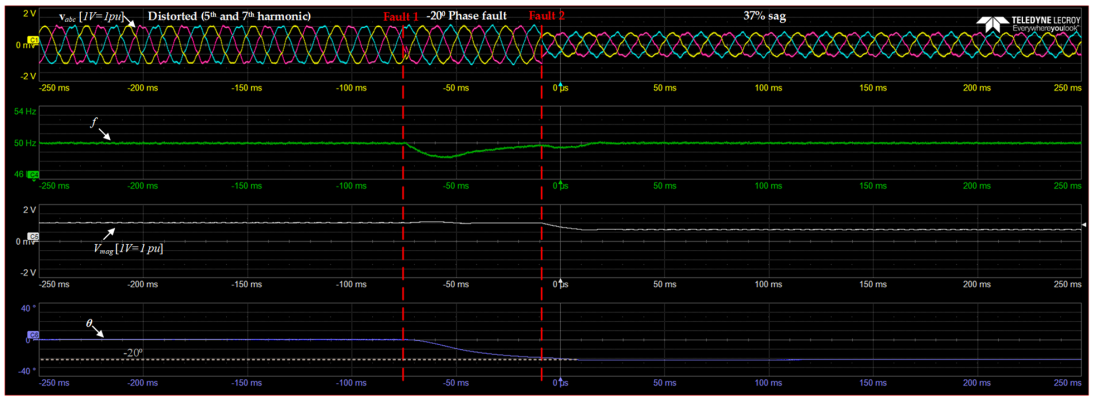

Figure 13. Experimental results for the real-time validation of the HIHDO-PMU under distortion, phase fault, and sag.

The response of the HIHDO-PMU was further validated for a new set of individual faults (such as a combination of harmonics, voltage sag, and frequency variations). The first individual fault was the introduction of 5% 7th, 3.5% 11th, 3% 15th, and 2% 17th harmonics, where the magnitude for each harmonic was based on the EN 50160 power quality standard. With normal initial conditions, the grid voltage distorted with harmonics (at the point marked with a red arrow) and the corresponding estimation of the voltage, frequency, and angle are presented in Figure 14. The harmonics were effectively compensated by the proposed HIHD-PMU, resulting in an accurate estimation of grid information, validating the accurate performance of the PMU for mitigating distortion in the input signals.

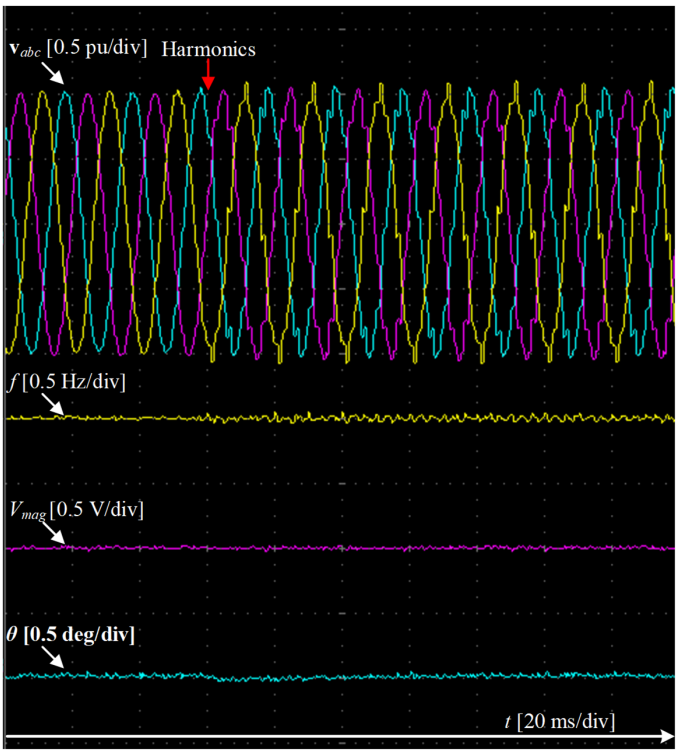

Figure 14. The response of the HIHDO-PMU to a set of harmonics.

Furthermore, a voltage sag event of 37% was applied where the voltage was changed from 1 p.u. to 0.63 p.u., and the response of the HIHDO-PMU was captured on an oscilloscope (Figure 15). The PMU estimated the current state of voltage in 10 ms. The fault slightly disturbed the frequency and phase estimation for a while, but the PMU overcame the fault and continued estimating the reference values (50 Hz for the frequency and 0 deg for the phase). Overshoots of 0.31 Hz and 1.03 deg were observed for the estimated frequency and phase, respectively, and settling times of 80 ms and 140 ms were observed for the estimated frequency and phase, respectively. The settling time was based on the reversion of the frequency from 50.031 Hz to 50 Hz and the phase from 1.03 deg to 0 deg. In practice, the variation window was large, so the actual settling time of the proposed PMU was considered as negligible. This showed that the proposed PMU can withstand the sag and continue predicting the frequency, phase, and magnitude of the grid voltage.

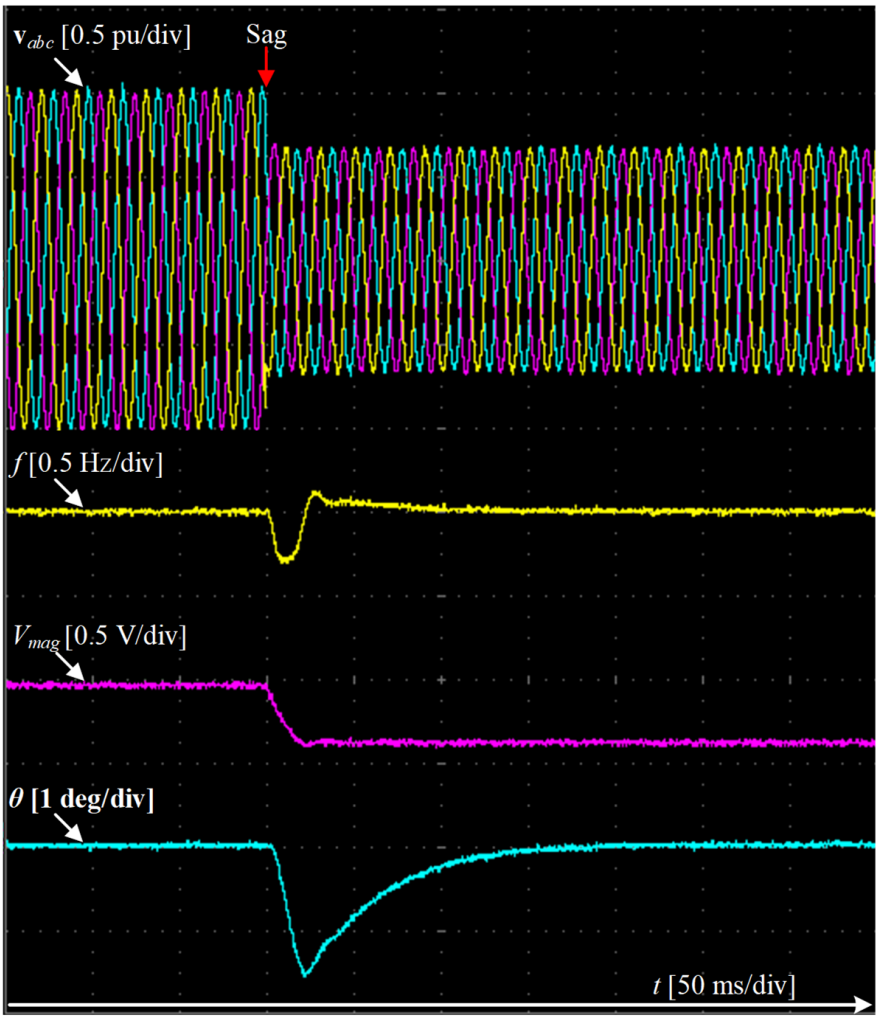

Figure 15. The response of the HIHDO-PMU to the voltage sag of 37%.

The response of the PMU was further validated for a frequency variation in the grid voltage. For this experiment, with a 50 Hz initial value, the operating frequency of the grid was changed from 50 Hz to 48 Hz, whereas the frequency of SRs (GPS signal) was unchanged (i.e., 50 Hz). The estimated frequency, phase angle, and magnitude responses are presented in Figure 16. The estimated quantities before fault were aligned with the reference value (i.e., 50 Hz frequency, 1 p.u. magnitude, and 0 deg phase). However, when the frequency fault occurred (marked in red), the PMU tracked the new reference for the frequency with a settling time of 100 ms (and an overshoot frequency of 1.05 Hz). A negligible notch was observed in the estimated magnitude, which reverted to 1 p.u.

Note that the frequency fault was clearly captured by the PMU angle estimation where it oscillated between 280 deg and 80 deg (covering a cycle of 360 degree). As the PMU angle was the difference between the PLL angle and the SR, a sudden decrease in the grid frequency would bring the PMU angle to negative values until a reset occurred. This validated the fast and accurate detection of the frequency using the proposed HIHDO-PMU.

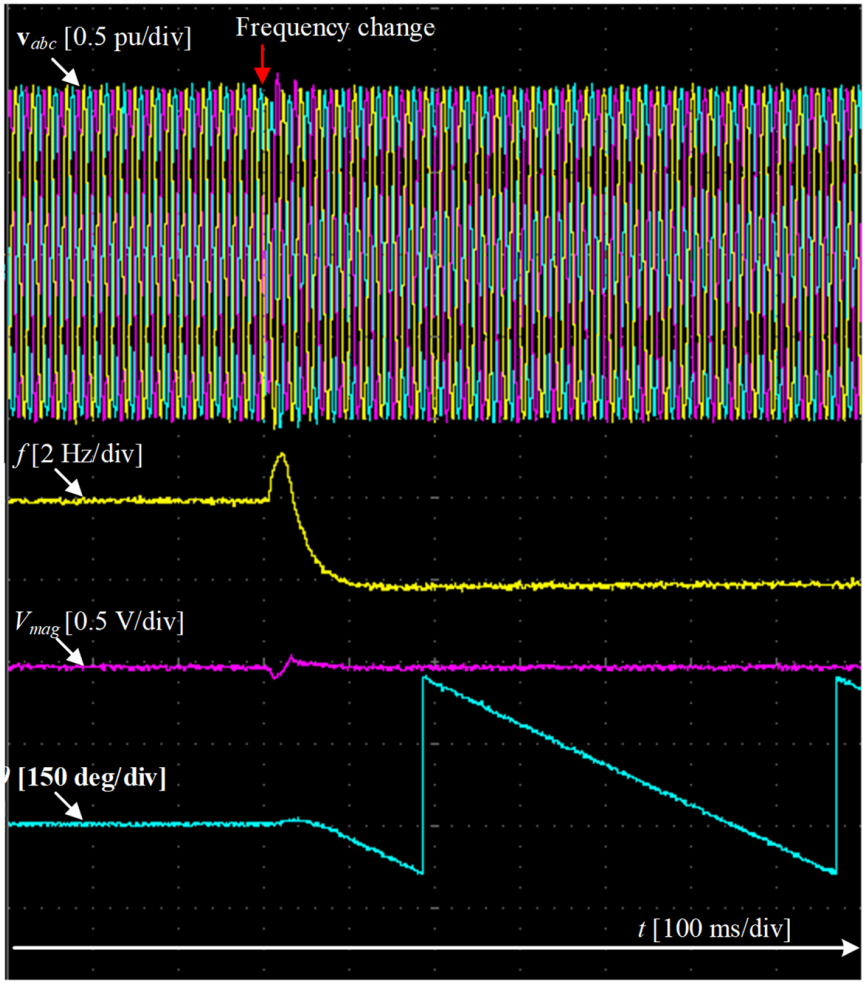

Figure 16. The response of the HIHDO-PMU to the frequency variation of −2 Hz (50 Hz to 48 Hz).

These experimental validations demonstrated the capability of the PLL to mimic the features and capabilities of the PMU under distorted and faulty grid conditions, resulting in the accurate estimation of frequency, phase, and amplitude. The use of the PLL thus complements existing algorithms embedded in the microcontroller for performing the extra functionalities of the PMU, thus saving implementation time and cost.

Additionally, the proposed HIHDO-PMU was compared to a DSOGI-based PMU such as the one suggested in [19]. The tuning parameters were similar for both the HIHDO- and DSOGI-PMUs. The first case introduced a combination of harmonics (5% 7th, 3.5% 11th, 3% 15th, and 2% 17th) and the two PMUs were compared, as shown in Figure 17. It was clearly seen that the HIHDO-PMU presented a better harmonic suppression capability compared to the DSOGI-PMU. The second comparison involved observing the estimation capabilities under harmonics and DC offset (10%), as shown in Figure 18 (for simplicity, only one phase of voltage is shown in green color). The DSOGI-PMU suffered from oscillations due to the presence of DC offset and harmonics and presented overshoots in the phase estimation and slower settling, whereas the HIHDO-PMU provided a fast and accurate estimation of the required grid quantities. Finally, the performance of the DSOGI-PMU was investigated for a frequency fault (where the input frequency was varied from 50 Hz

to 52 Hz), and the response of DSOGI is presented in Figure 19. Comparing two PMUs (results in Figures 16 and 19) showed that the SOGI-PMU suffered from a high-frequency overshoot (i.e., 6 Hz) and requires 200 ms to detect the change in the frequency and the corresponding variations in the estimated phase (which showed that the system frequency was different than that of the SR). The three cases considered showed the HIHDO-PMU is a better candidate for the analysis and control of power system operation as it presents a fast and robust estimation performance under distorted and faulty grid conditions.

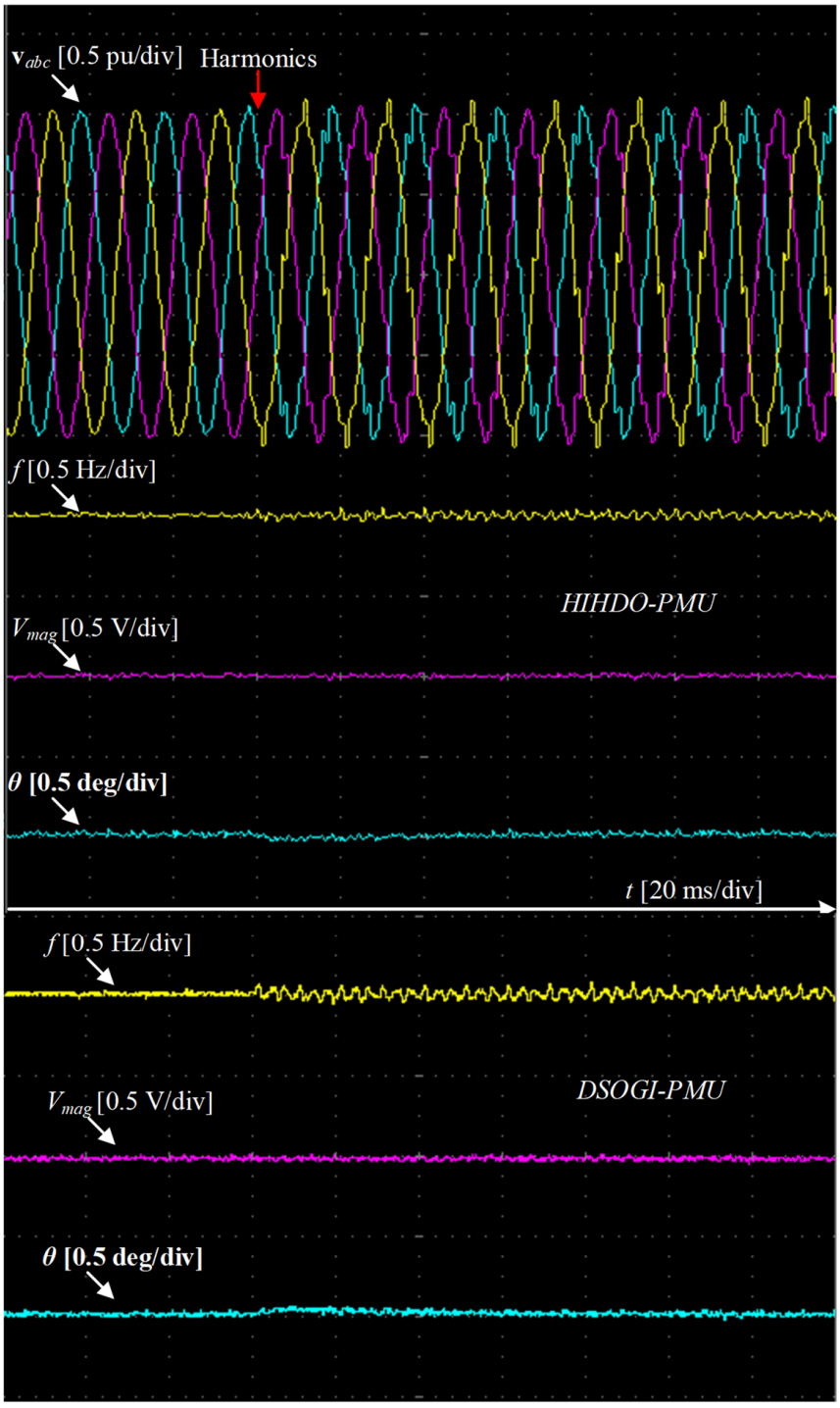

Figure 17. Performance comparison of the HIHDO- and dual second-order generalized integrator (DSOGI)-PMUs under harmonics.

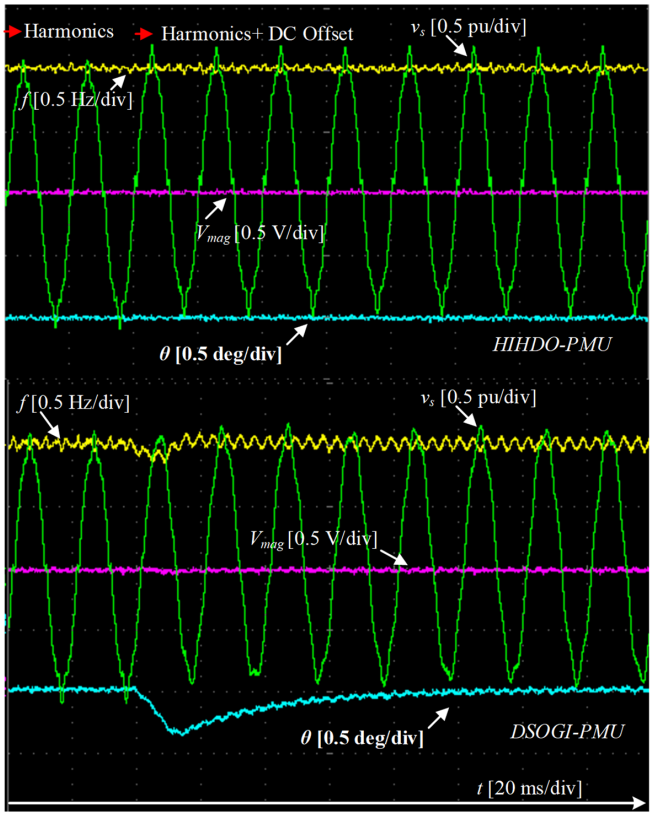

Figure 18. Performance comparison of the HIHDO- and DSOGI-PMUs under harmonics and DC offset.

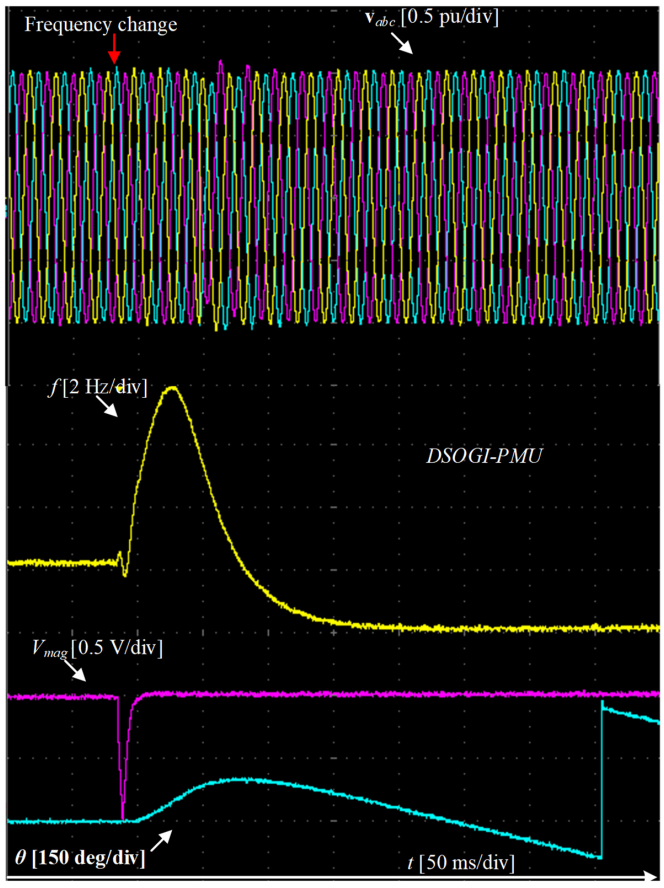

Figure 19. Response of the DSOGI-PMU under frequency variations.

5. Kundur's Two-Area System

The impact of the HIHDO-PMU was analyzed by assessing its performance in a power system with several generators and load buses. The system under consideration was the Kundur's two-area system defined and introduced in [27] and is now a standard model for analyzing the dynamic phenomena in power systems [28,29]. It comprises 11 buses, four identical generators, and two areas, as shown in Figure 20. The two areas are connected through a weak tie link, and system parameters are given in [27].

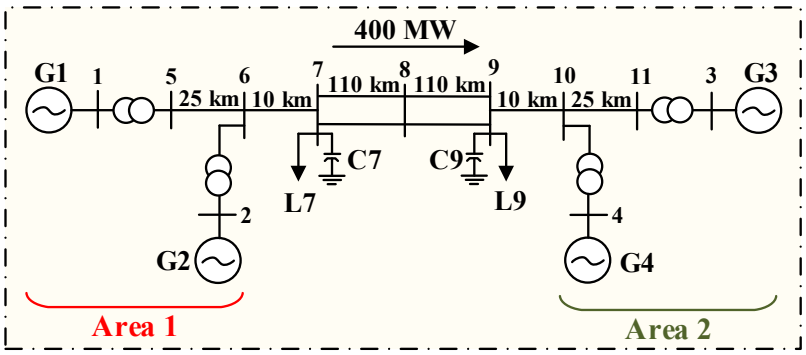

Figure 20. Kundra's two-area system.

Two PMUs are connected to bus 1 to measure and analyze the voltage and current separately. Under normal initial conditions, a three-phase to ground fault occurs at bus 7 for 2 s with a duration of 0.1 s. Following the fault clearance, a new steady state is presented. The voltages and currents of PMUs accurately estimate the varying phasors, predicts the frequency and magnitude and are robust to grid fault, as shown in Figure 21. The accurate performance of the suggested HIHDO-PMU was analyzed by measuring the three-phase active power at bus 1 using the estimated PMU quantities, such as the voltage angle, current angle, and voltage and current magnitudes, given in Figure 22. It is obvious that the estimated active power using the HIHDO-PMU clearly followed the reference power of G1 in the network. This verified the accurate performance of the HIHDO-PMU for a power system.

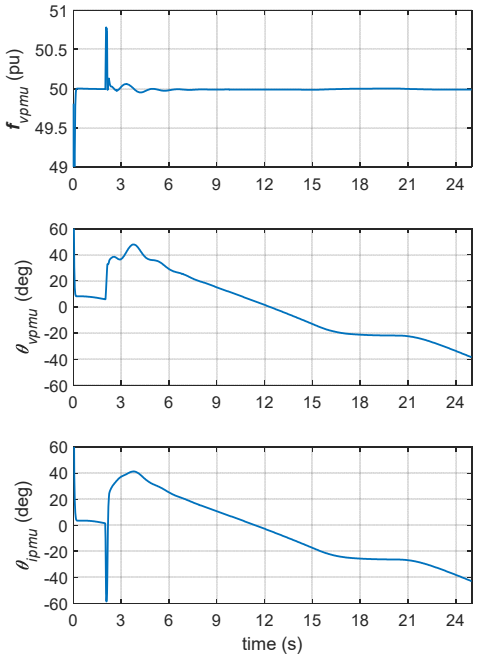

Figure 21. The HIHDO-PMU measurement for generator 1.

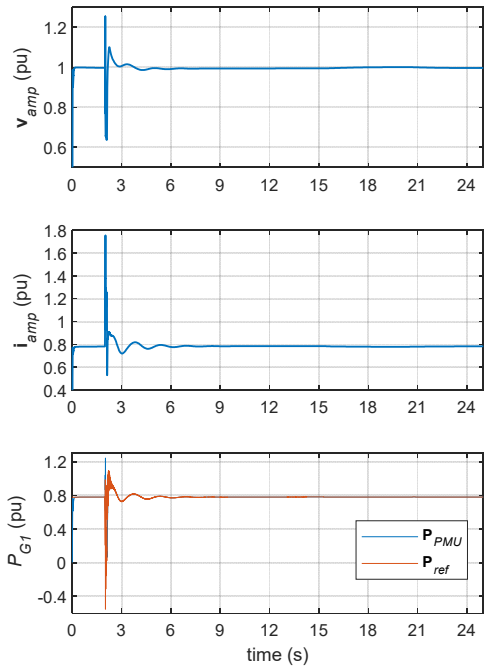

Figure 22. The estimated voltage amplitude, current amplitude, and generator G1 power.

6. Conclusions

This paper investigates the use of the PLL for PMU functionalities, and it was shown that the proposed HIHDO-PMU performed accurately with fast dynamics and lower overshoots. Conversely, the αβEPMAFPMU performed better for magnitude estimation but had undesired long settling times. The dqPLL performed well for normal conditions, whereas DNαβPMU had a lower overall performance. It is worth mentioning that the HIHDO-PMU was less complex compared to the DNαβPLL. Additionally, the HIHDO PMU was compared to the DSOGI-based PMU under various grid conditions, which also showed the HIHDO-PMU presented a fast and robust estimation performance under distorted and faulty grid conditions. The performance analysis and benchmarking under grid faults showed that the PLL is a suitable candidate to be used for PMUs, and existing systems with embedded PLL in microcontrollers can be modified and used to perform extra functionalities of PMUs. Furthermore, the use of the proposed HIHDO-PMU was verified by using it in the Kundur's two-area power system to measure the voltage and current (and power) from a generator under grid fault. The estimated active power using the HIHDO-PMU output quantities aligned with the known reference power of G1 in the network, thus verifying the accurate performance of the HIHDO-PMU for monitoring the power system. Future work includes analyzing the performance of networks using multiple PMUs and faults at various locations.

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